

FIG. 1

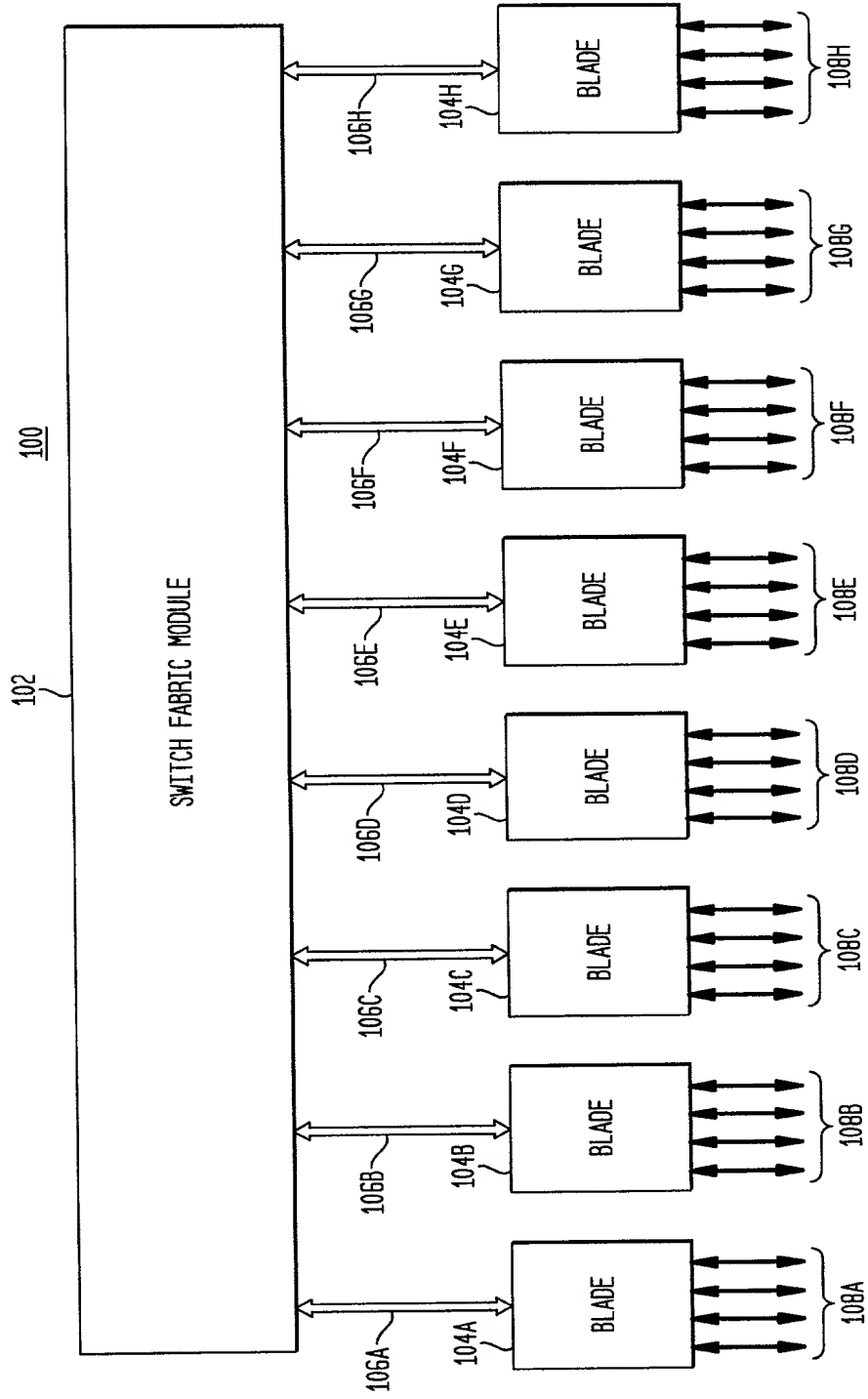


FIG. 2

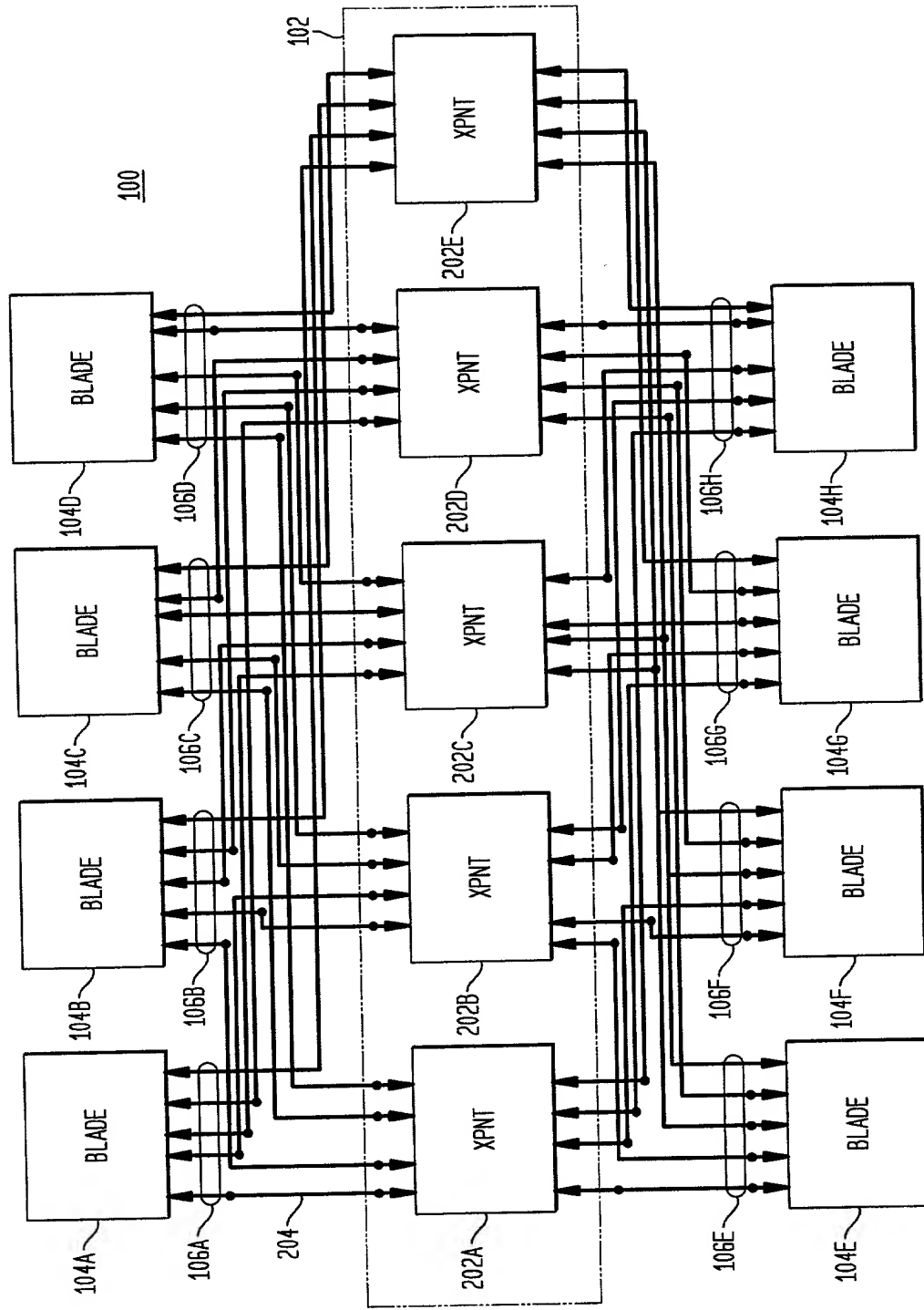


FIG. 3A

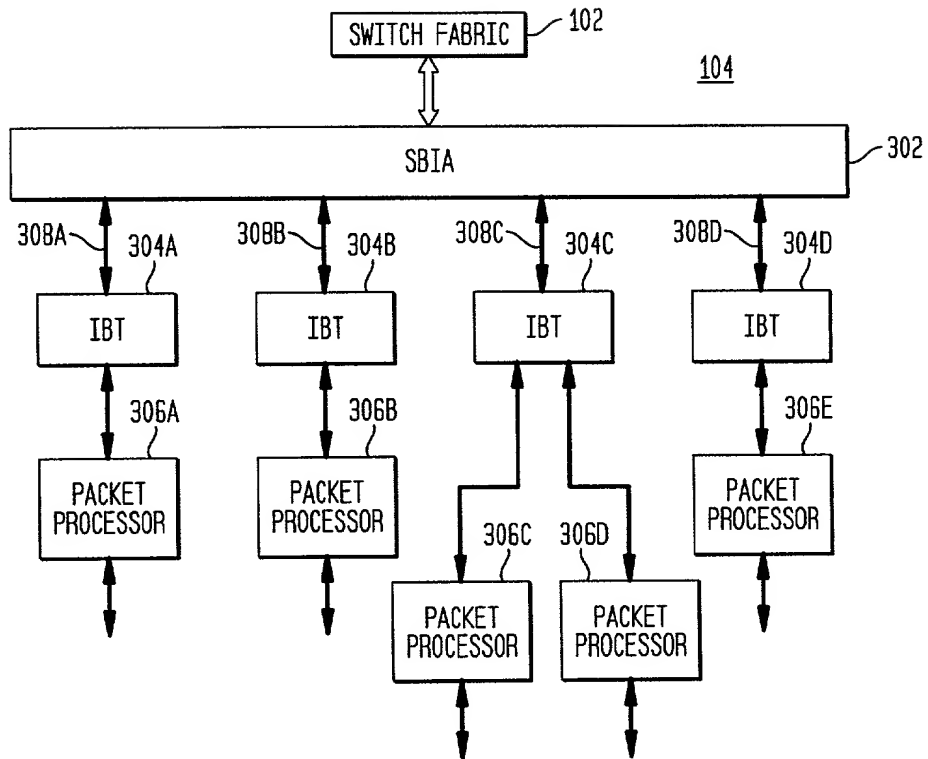


FIG. 3B

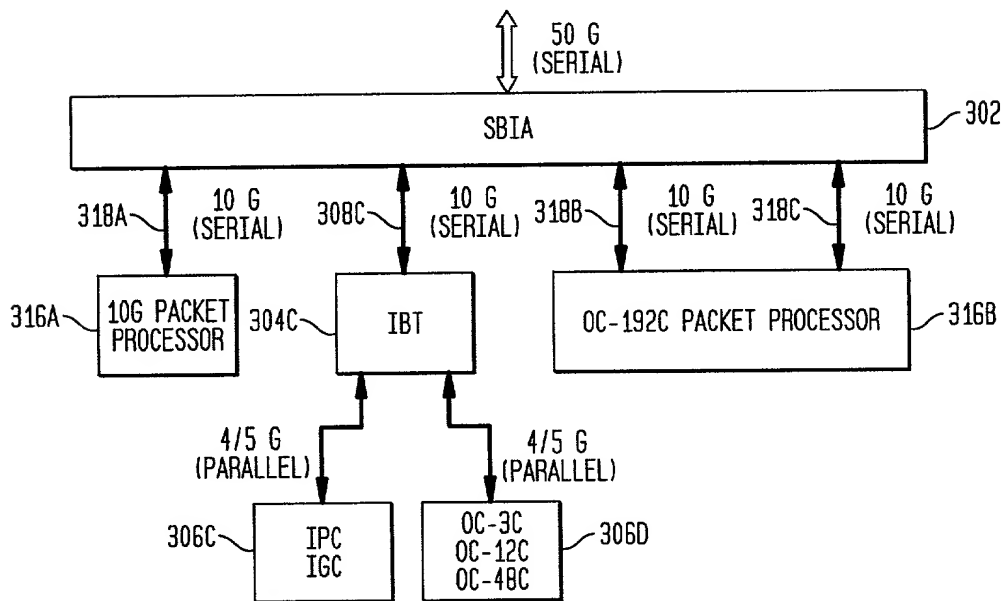


FIG. 4

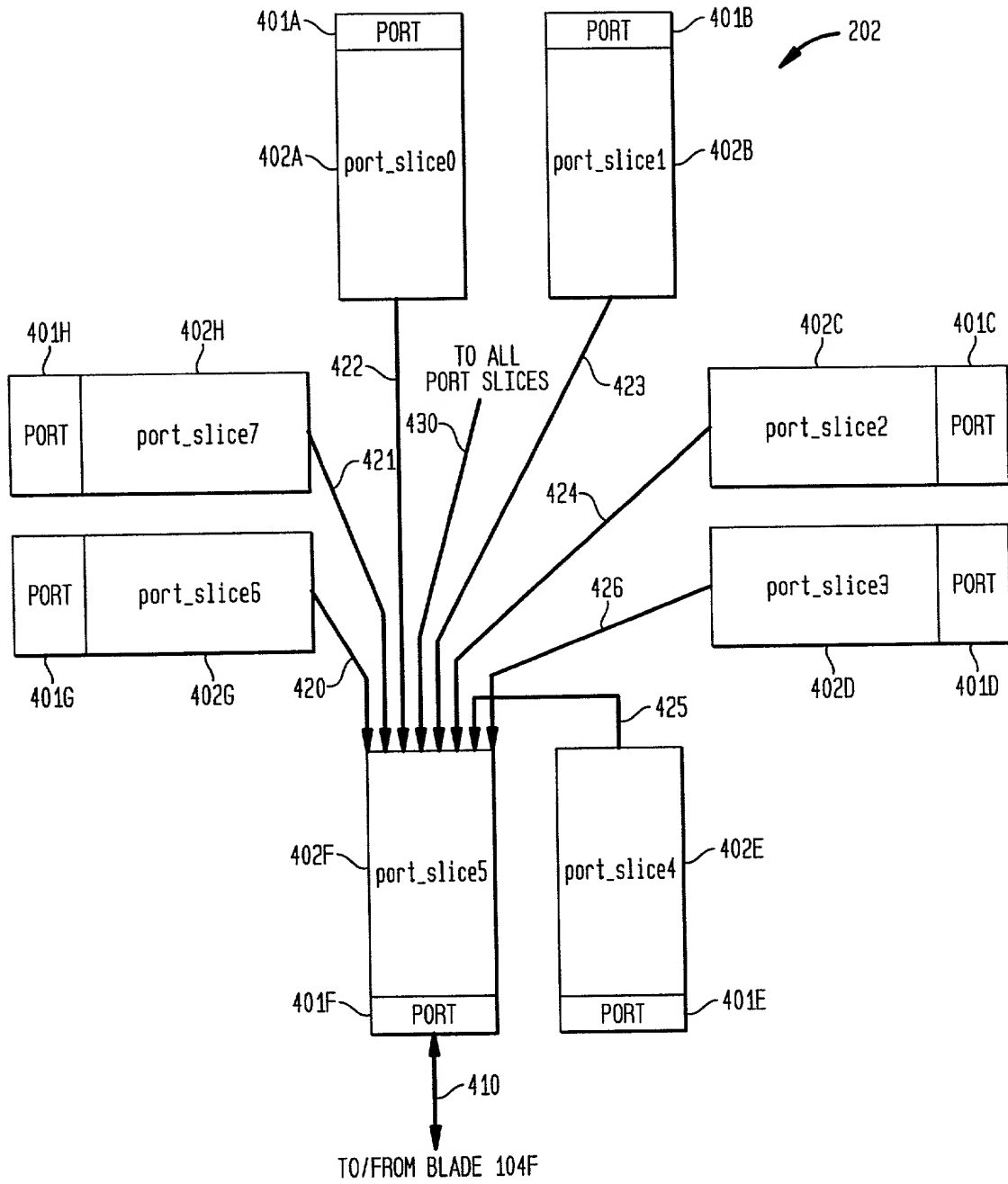


FIG. 5

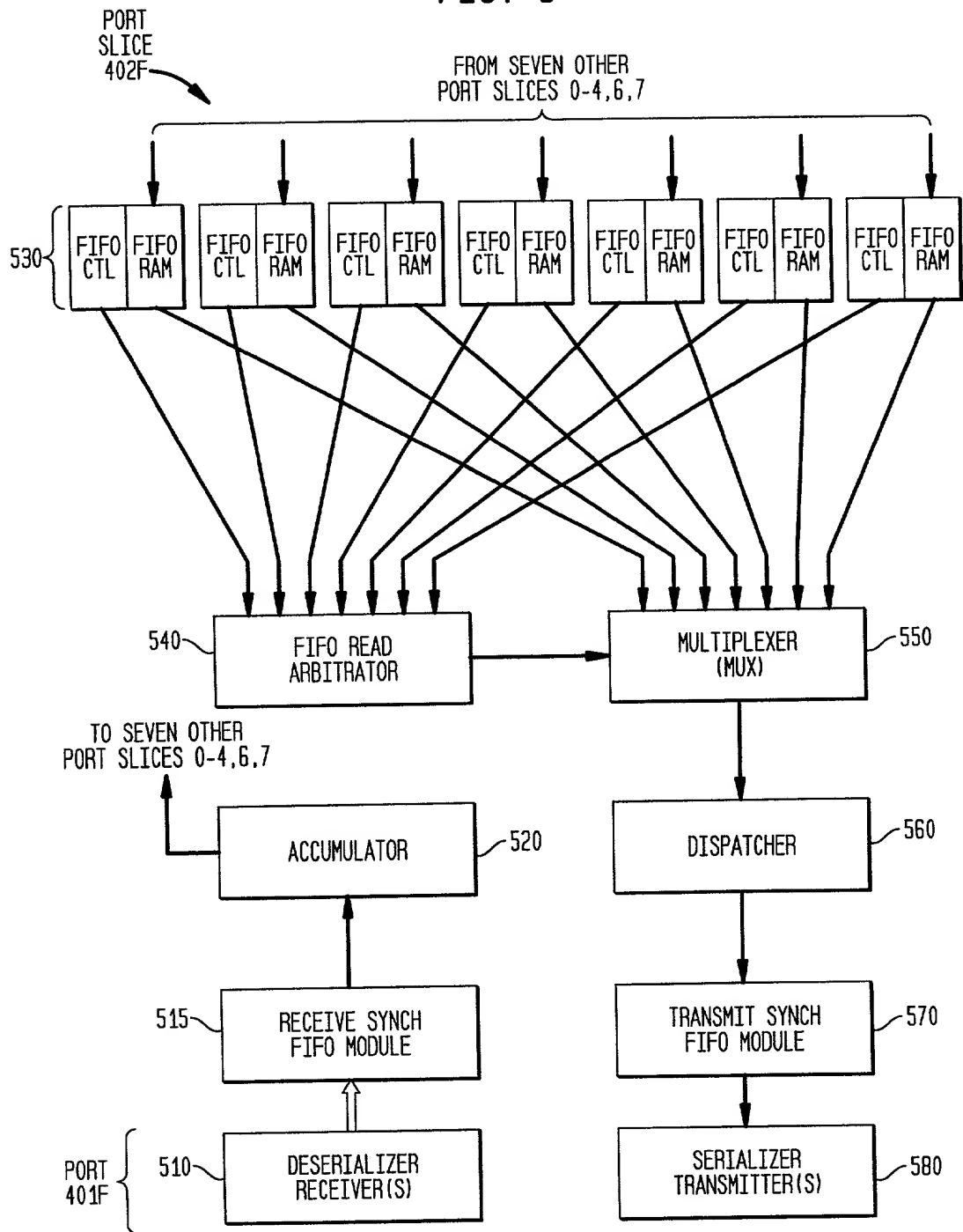


FIG. 6

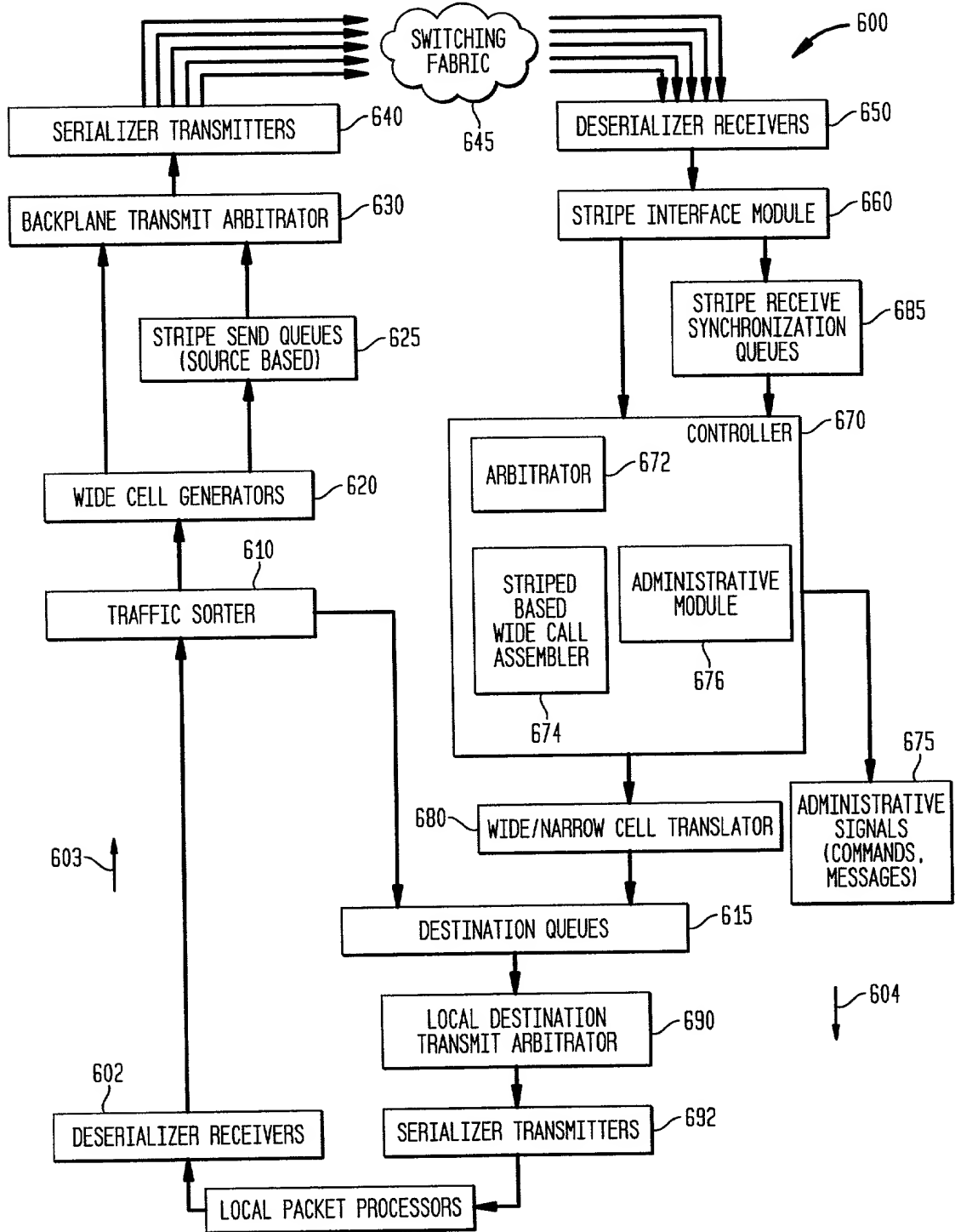


FIG. 7

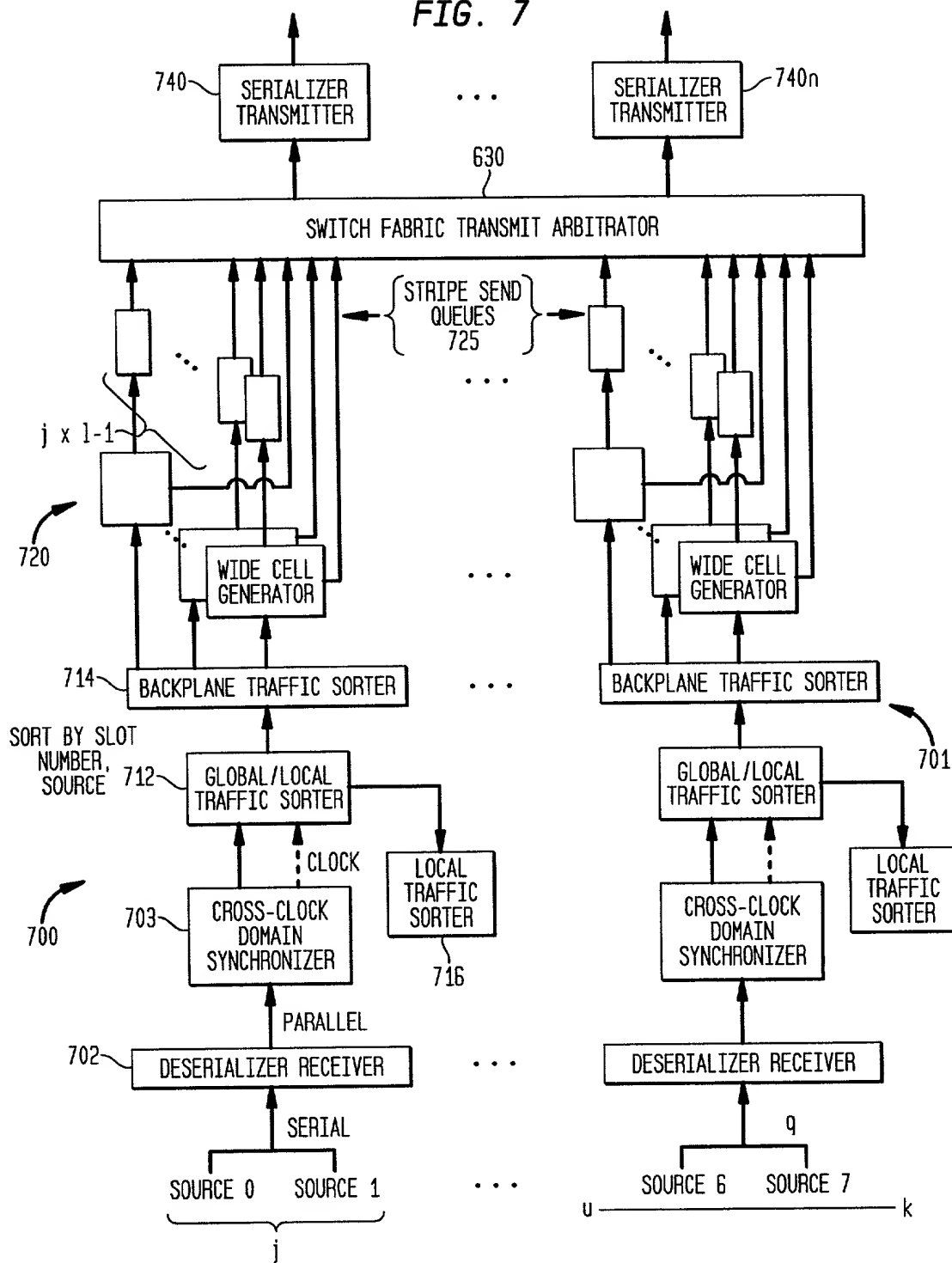
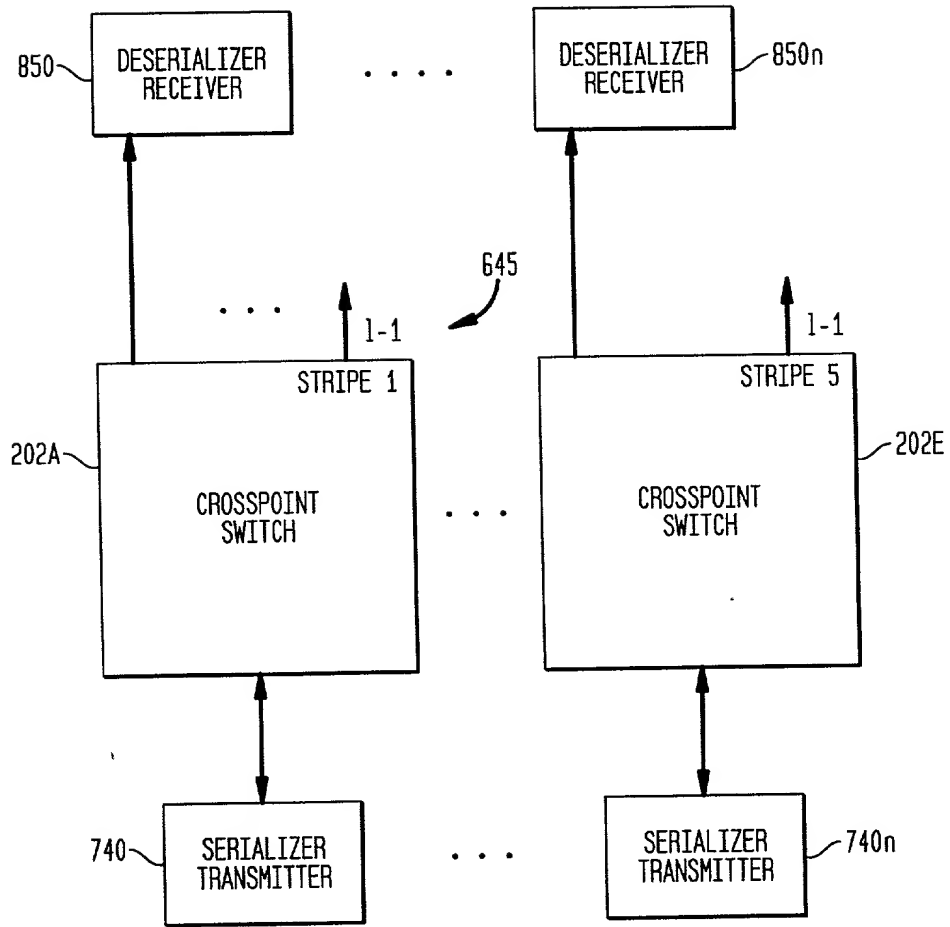


FIG. 8



09990000 11601



FIG. 9

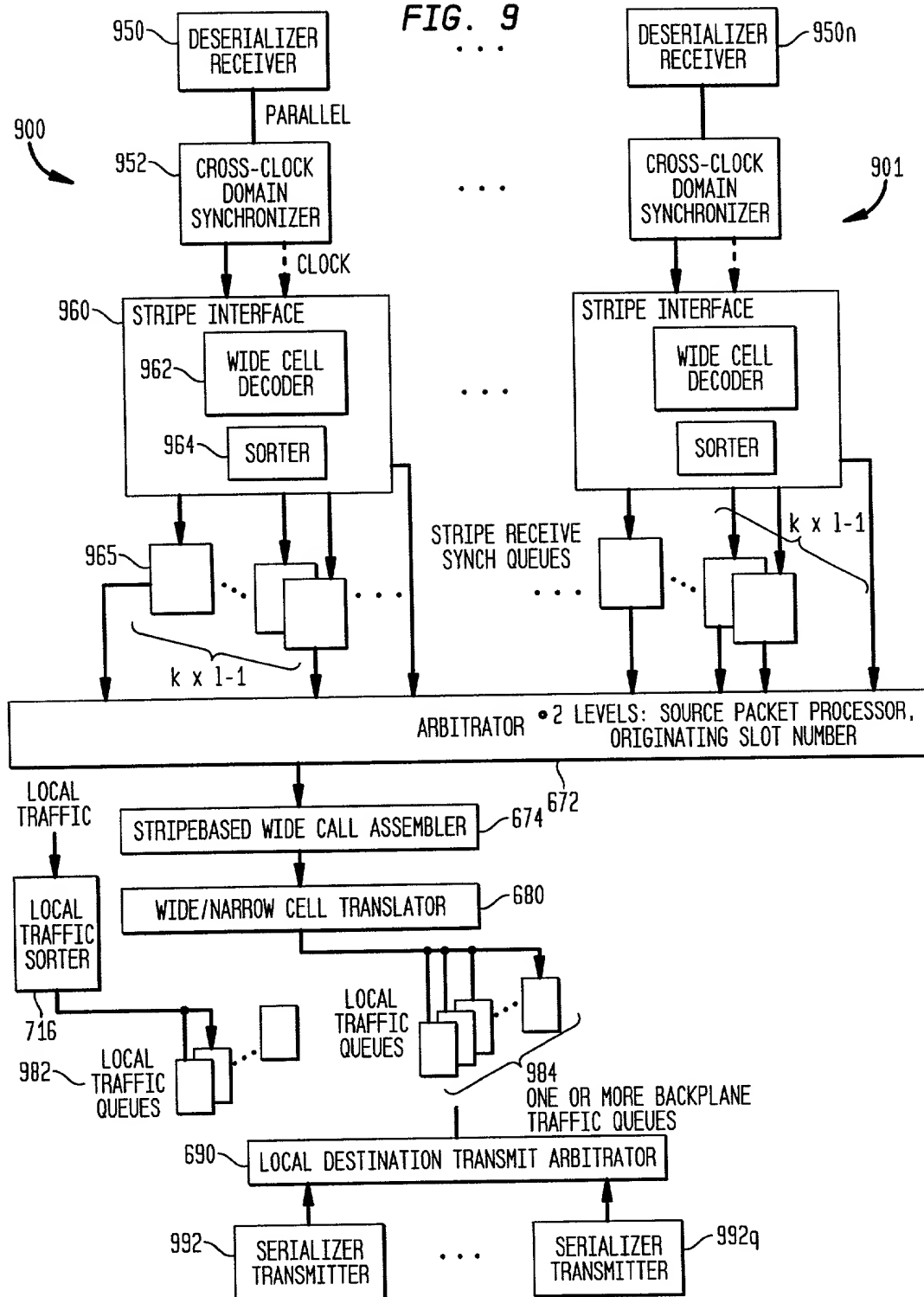


FIG. 10

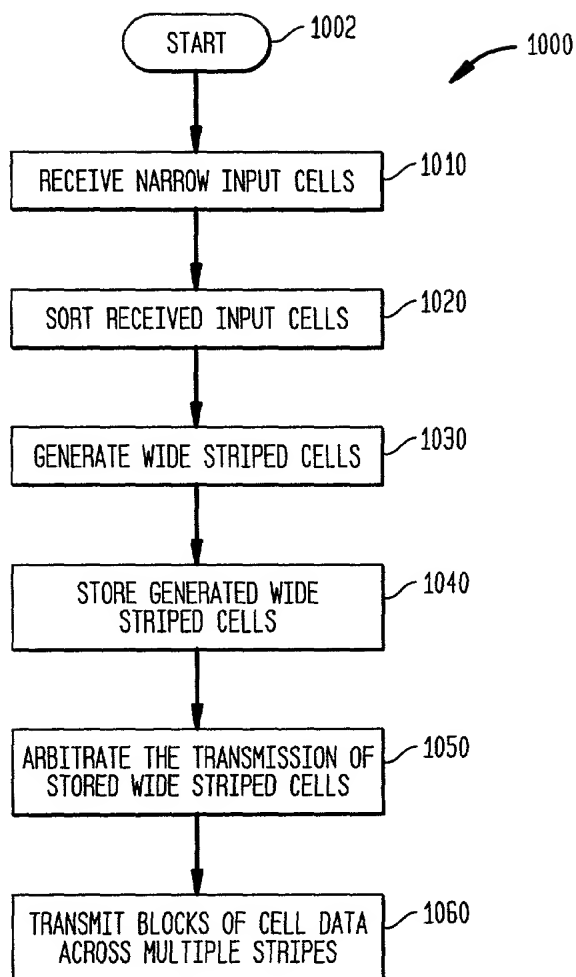


FIG. 11

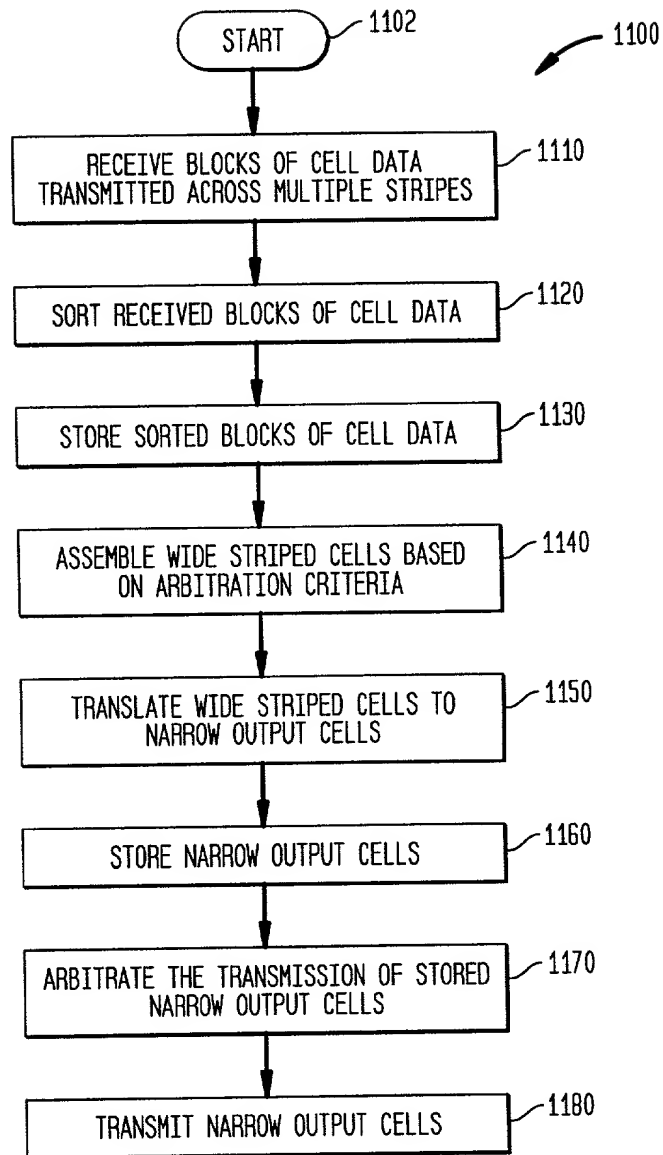
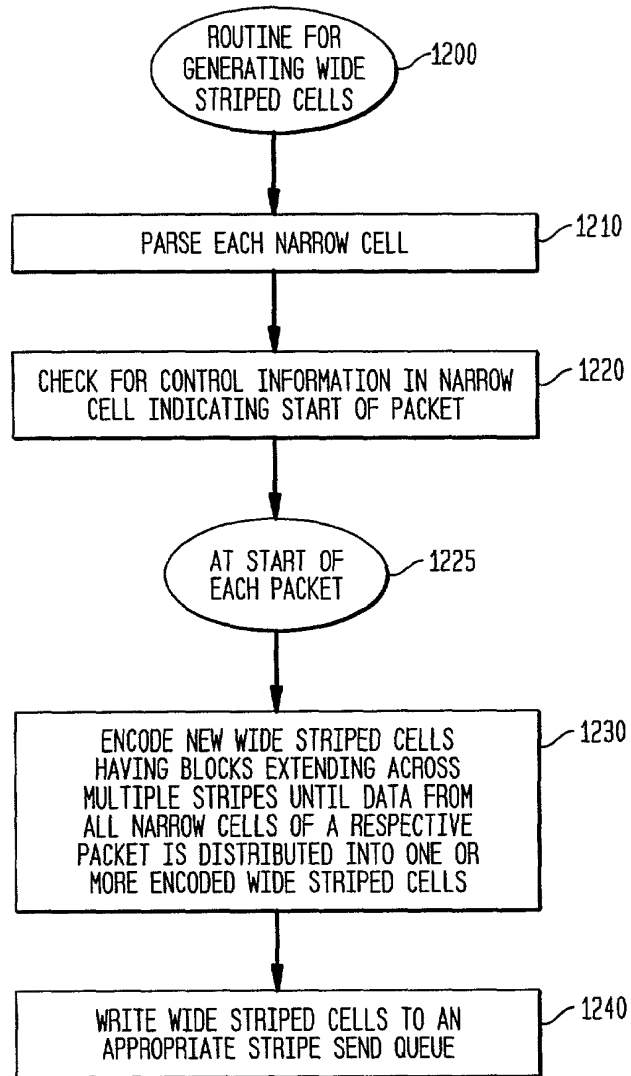


FIG. 12



09988066 11601

FIG. 13

LANE 0	LANE 1	LANE 2	LANE 3
CONTROL INFORMATION	STATE INFORMATION	RESERVED	RESERVED
D0	D1	D2	D3
D4	D5	D6	D7
D8	D9	D10	D11
D12	D13	D14	D15
⋮	⋮	⋮	⋮
D28	D29	D30	D31

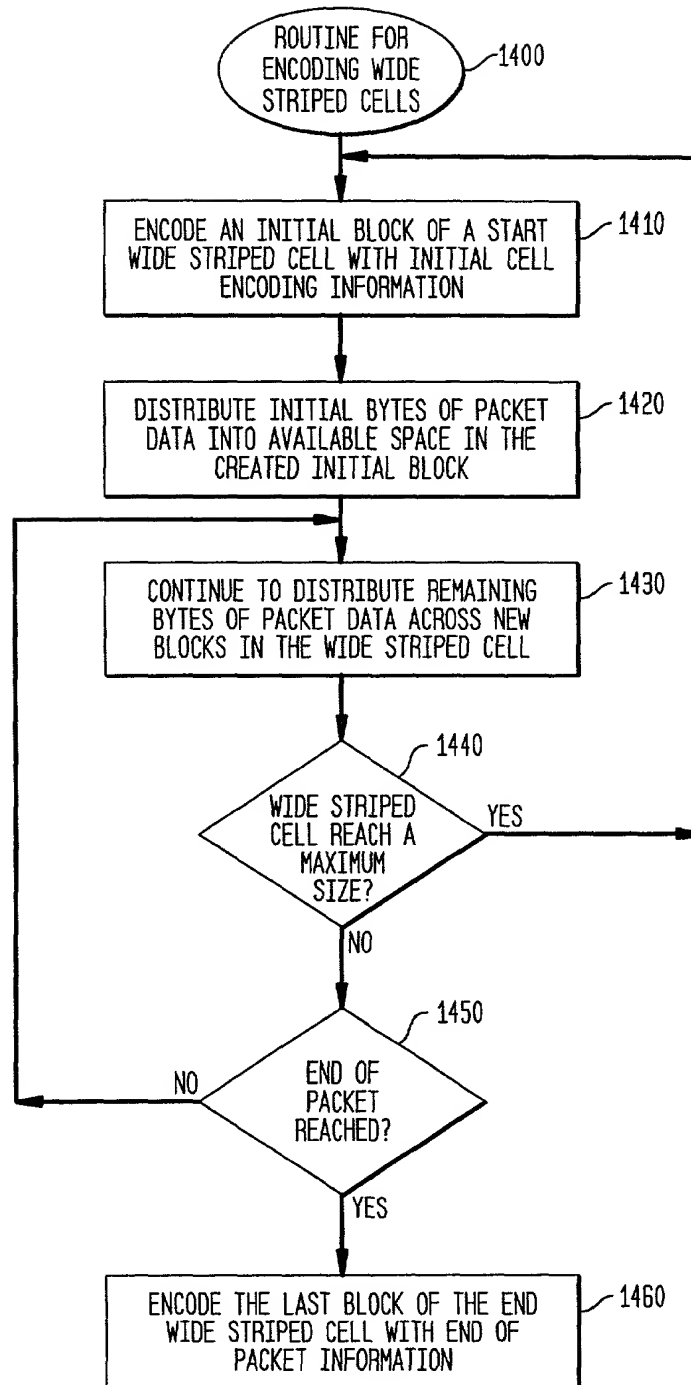
1300

1310

STATE INFORMATION	
NAME	DESCRIPTION
SLOT NUMBER	DESTINATION SLOT NUMBER WHERE CELL DATA BEING SENT
PAYLOAD STATE	RESERVED, SOP, DATA, ABORT
SOURCE OR DESTINATION PACKET PROCESSOR IDENTIFIER	ENCODED NUMBER IDENTIFYING A SOURCE OR DESTINATION PACKET PROCESSOR
RESERVED	RESERVED

09988066-111501

FIG. 14



0988066-11601

FIG. 15A

CYCLE	STRIPE 1				STRIPE 2				STRIPE 3				STRIPE 4				STRIPE 5			
	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3
1	K0	STATE	D0	D1	K0	STATE	D2	D3	K0	STATE	D4	D5	K0	STATE	D6	D7	K0	STATE	RES	RES
2	D8																			D27
3	D28																			D47
4	D48																			D67
5	D68																			D87
6	D88																			D107
7	D108																			D127
8	D128																			D147

1500

FIG. 15B

STATE INFORMATION	
NAME	DESCRIPTION
SLOT NUMBER	DESTINATION SLOT NUMBER FOR BIA TO CROSSPOINT SWITCH DIRECTION SOURCE SLOT NUMBER FOR CROSSPOINT SWITCH TO BIA DIRECTION
PAYLOAD STATE	ENCODED PAYLOAD STATE INFORMATION (RESERVED, SOA, DATA, ABORT)
RESERVED	RESERVED

FIG. 15C

END OF PACKET ENCODING INFORMATION

1. EOP DURING CYCLE 1 (ie. DURING TRANSMISSION OF STATE INFORMATION)

1	K0	state	D0	D1	K0	state	D2	D3	K0	state	K1	K1	K0	state	RES	RES
---	----	-------	----	----	----	-------	----	----	----	-------	----	----	----	-------	-----	-----

NOTE THAT THE K0, STATE, AND RESERVED BYTES ARE ALL PRESERVED, AS IN ANY OTHER CYCLE 1 TRANSMISSION. THE K1 CHARACTER IS TREATED AS DATA

2. EOP DURING CYCLE n (n!=0)

1	K0	state	D0	D1	K0	state	D2	D3	K0	state	D4	D5	K0	state	D6	D7	K0	state	RES	RES
2	D8																			D27
3	D28				D32	D33	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1

3. EOP AT BLOCK BOUNDARY DURING CYCLE n (n!=8)

1	K0	state	D0	D1	K0	state	D2	D3	K0	state	D4	D5	K0	state	D6	D7	K0	state	RES	RES
2	D8																			D27
3	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1

NOTE THAT WHEN n>0, THE BLOCK BOUNDARY FOR DATA IS IN LANE 3 STRIPE 5. HOWEVER, FOR n=0. THE BLOCK BOUNDARY FOR DATA IS IN LANE 3 OF STRIPE 4.

4. EOP at cell boundary

6	D88																			D107
7	D108																			D127
8	D128																			D147

1	K0	state	K1	K1	K0	state	K1	K1	K0	state	K1	K1	K0	state	RES	RES
---	----	-------	----	----	----	-------	----	----	----	-------	----	----	----	-------	-----	-----



FIG. 15D

CYCLE	STRIPE 1				STRIPE 2				STRIPE 3				STRIPE 4				STRIPE 5			
	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3
1	K0	P1	D0	D1																
2	D8			D11																
3	D28			D31	K0	P1	D2	D3												
4	D48			D51	D12			D15					K0	P1	D6	D7				
5	D68			D71	D32			D35					D20			D23				
6	D88			D91	D52			D55	K0	P1	D4	D5	D40			D43				
7	D108			D111	D72			D75	D16			D19	D60			D63	K0	P1	RES	RES
8	D128			D131	D92			D95	D36			D39	D80			D83	D24			D27

09938066-111001

FIG. 16

CYCLE	STRIPE 1				STRIPE 2				STRIPE 3				STRIPE 4				STRIPE 5			
	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3	L0	L1	L2	L3
1	K0	SS1	D0	D1	K0	SS6	D151	D152	K0	SS2	D4	D5	K0	SS3	D6	D7	K0	SS7	RES	RES
2	D8			D11	D161	D162	D163	K1	D16			D19	D20			D23	D320			D323
3	D28			D31	K0	SS2	D2	D3	D36			D39	D40			D43	D340			D343
4	D48			D51	D12			D15	D56			D59	K0	SS4	D6	D7	D360			D363
5	D68			D71	D32			D35	D76	K1	K1	K1	D20			D23	D380			D383
6	D88			D91	D52			D55	K0	SS3	D4	D5	D40			D43	K1	K1	K1	K1
7	D108			D111	D72			D75	D16			D19	D60			D63	K0	SS5	RES	RES
8	D128			D131	K0	SS5	D2	D3	D36			D39	D80	K1	K1	K1	D24			D27
9	K0	SS4	D0	D1	D12			D15	K0	SS6	D153	D154	K0	SS2	D6	D7	D44			D47
10	D8			D11	D32			D35	K1	K1	K1	K1	D20			D23	D64			D67
11	D28			D31	D52			D55	K0	SS7	D300	D301	D40			D43	K0	SS1	RES	RES
12	D48			D51	K0	SS1	D2	D3	D312			D315	D60			D63	D24			D27
13	D68			D71	D12			D15	D332			D335	K1	K1	K1	K1	D44			D47
14	K0	SS7	D296	D297	D32			D35	D352			D355	K0	SS6	D155	D156	D64			D67
15	D304			D307	D52			D55	D372			D375	K1	K1	K1	K1	D84			D87
16	D324			D327	D72			D75	K1	K1	K1	K1	K0	SS1	D6	D7	D104			D107
17	D344			D347	D82			D85	K0	SS5	D4	D5	D20			D23	D124			D127
18	D364			D367	D112			D115	D36			D39	D40			D43	D144			D147
19	K1	K1	K1	K1	D132			D135	D36			D39	D60			D63	D0	SS3	RES	RES
20	K0	SS6	D149	D150	K0	SS7	D298	D299	D56			D59	D80			D83	D24			D27
21	D157			D160	D308			D311	K0	SS1	D4	D5	D100			D103	D44	D45	K1	K1
22	K0	SS1	K1	K1	D328			D331	D16			D19	D120			D123	K0	SS2	RES	RES
23	K0	SS3	D0	D1	D348			D351	D36			D39	D140			D143	D24			D27
24	D8			D11	D368			D371	D56			D59	K0	SS7	D302	D303	D44			D47

 GREEN
  YELLOW
  ORANGE
  BLUE
  RED
  RUST
  PINK

0998066-11601

FIG. 17

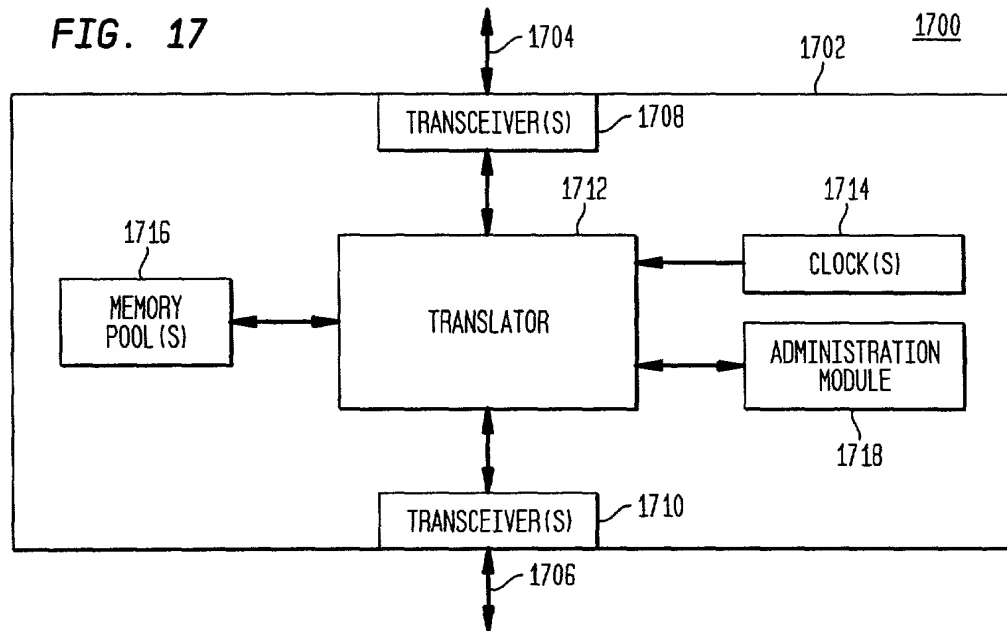
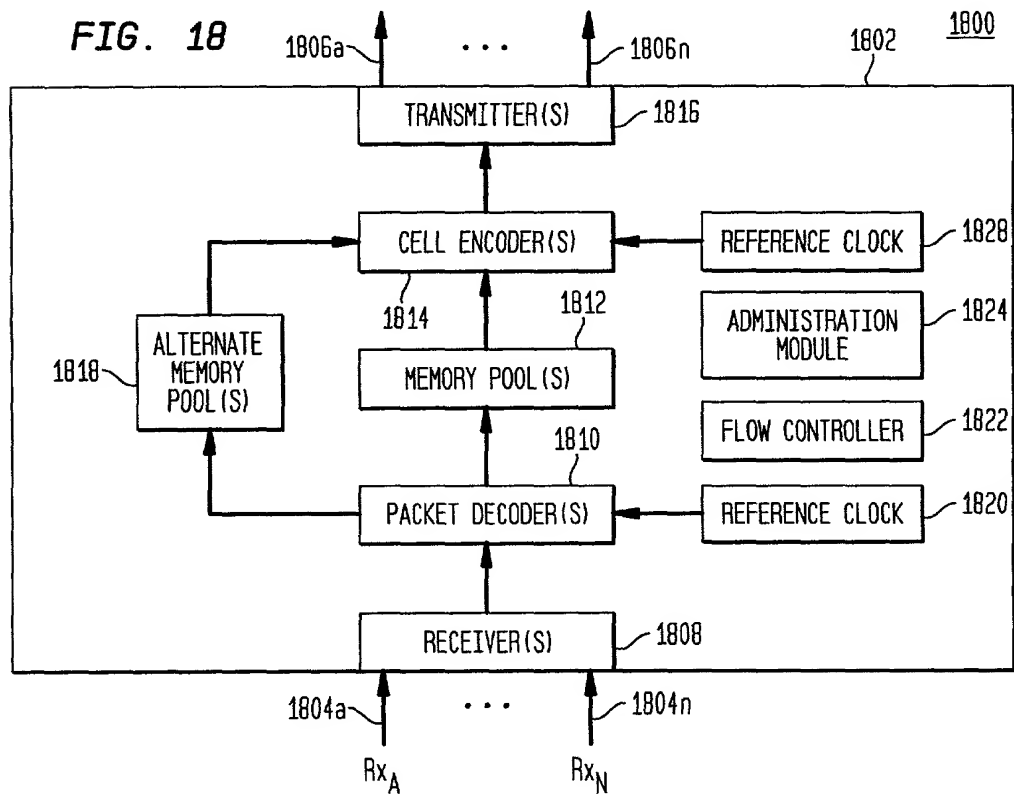
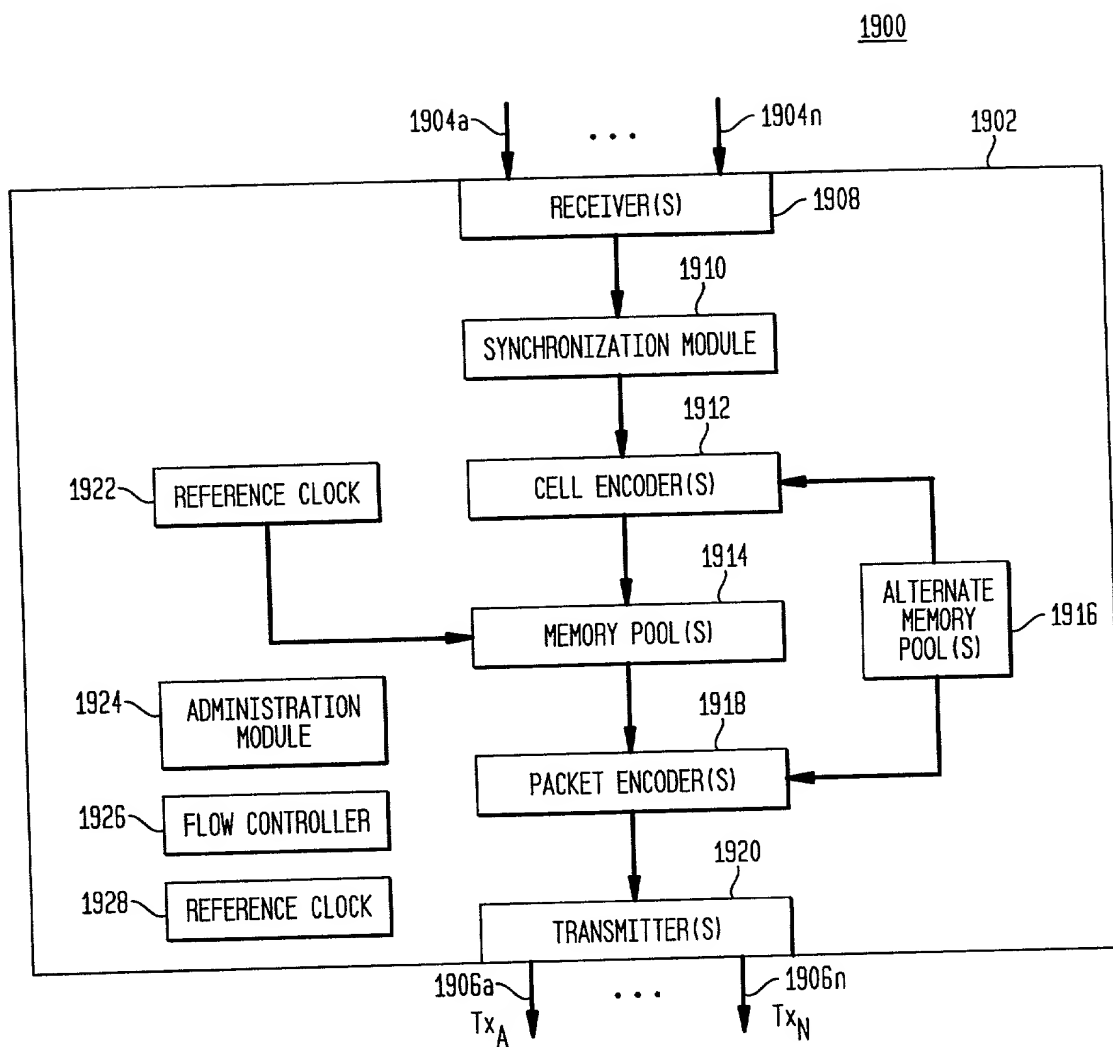


FIG. 18



[illegible]

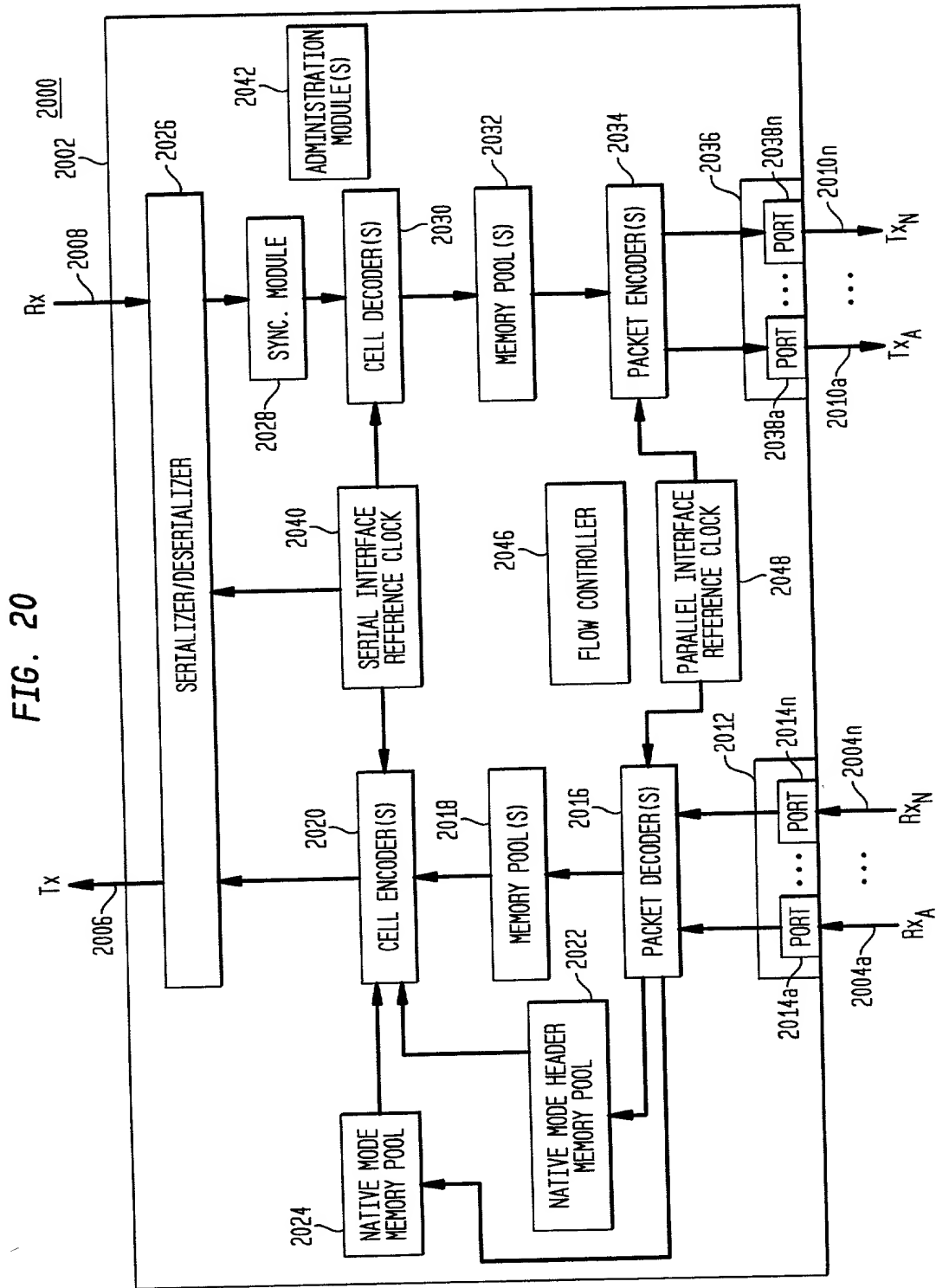




FIG. 21B

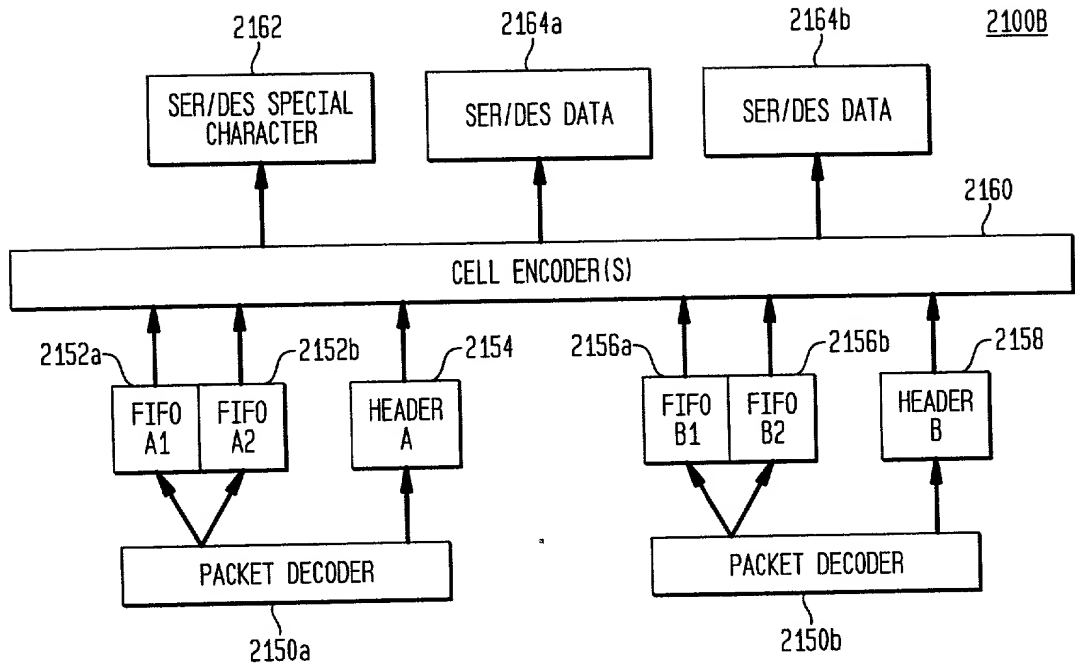


FIG. 21C

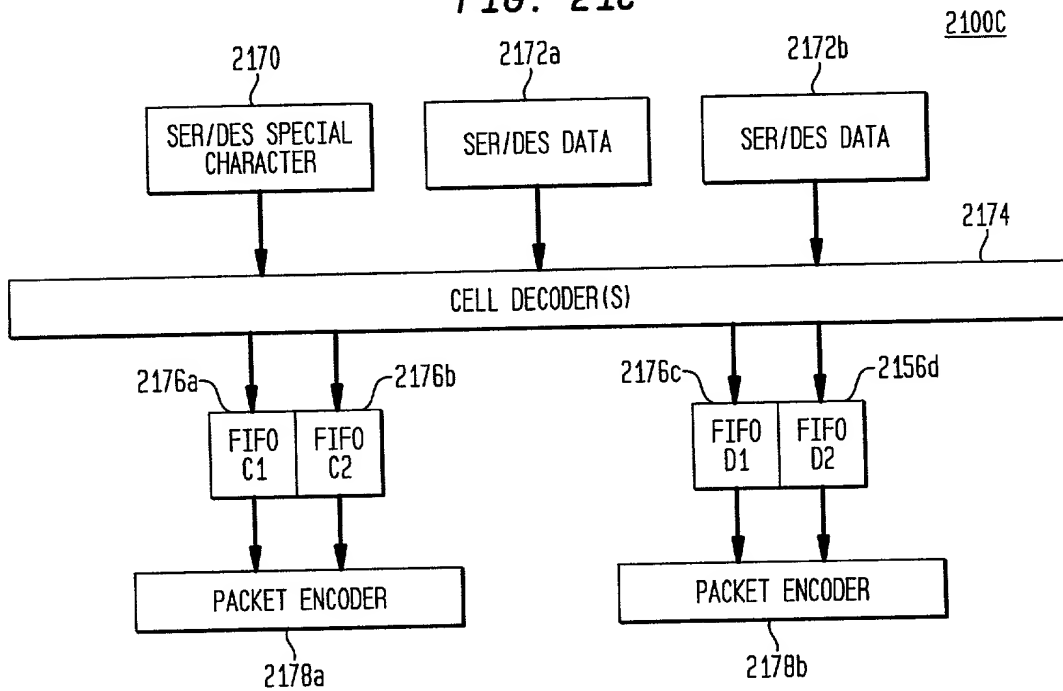


FIG. 21D

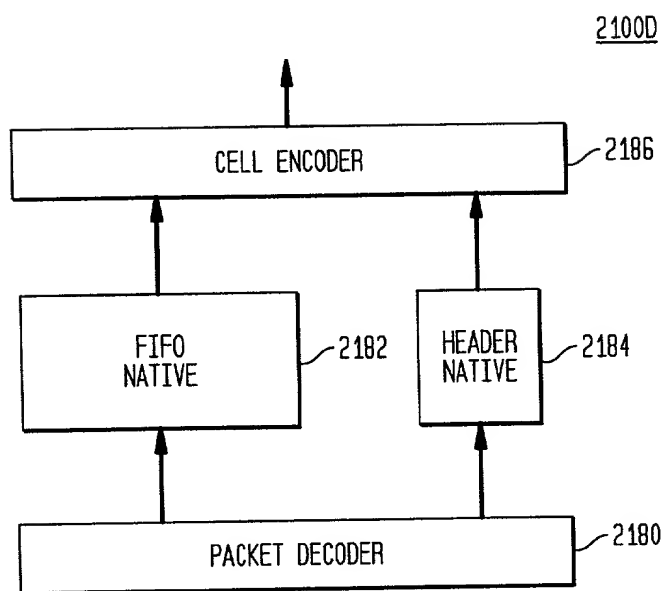




FIG. 21E

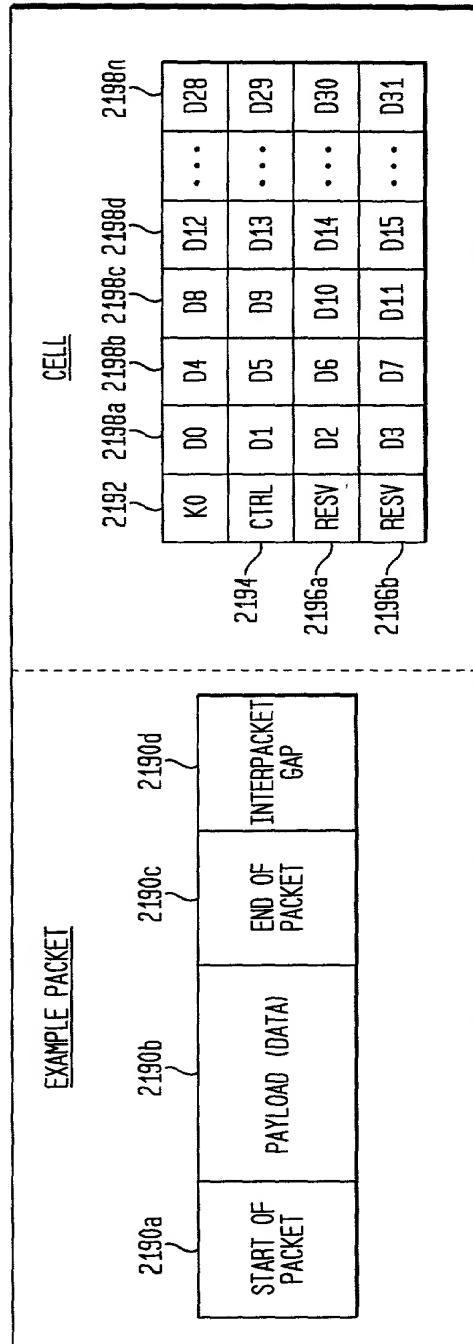
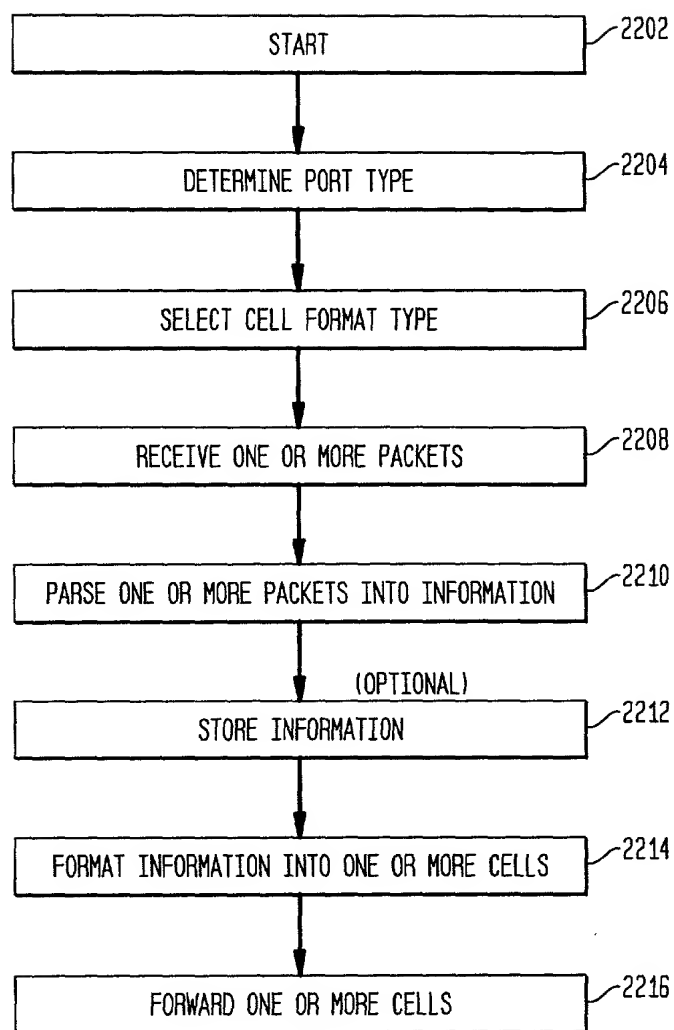


FIG. 22



09938065 111501

FIG. 23A

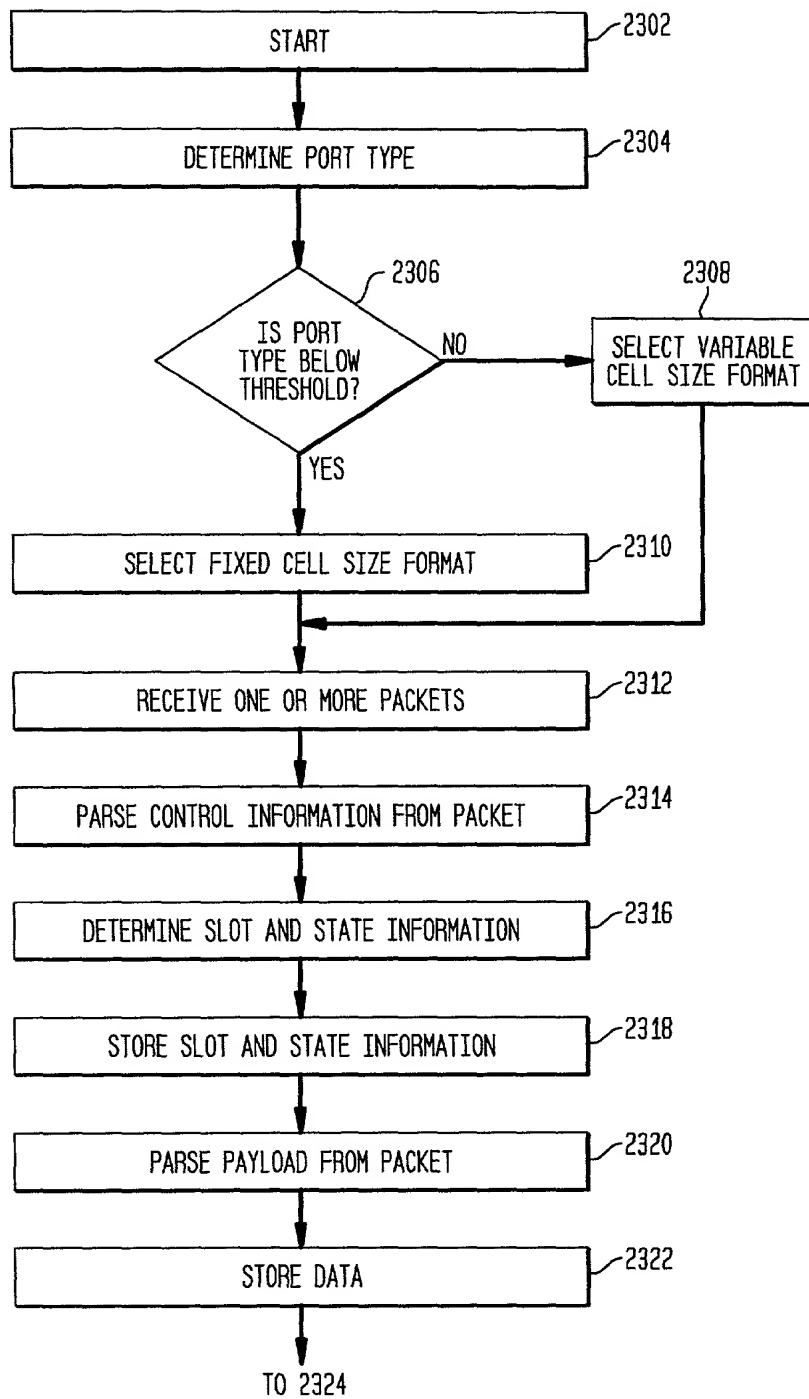
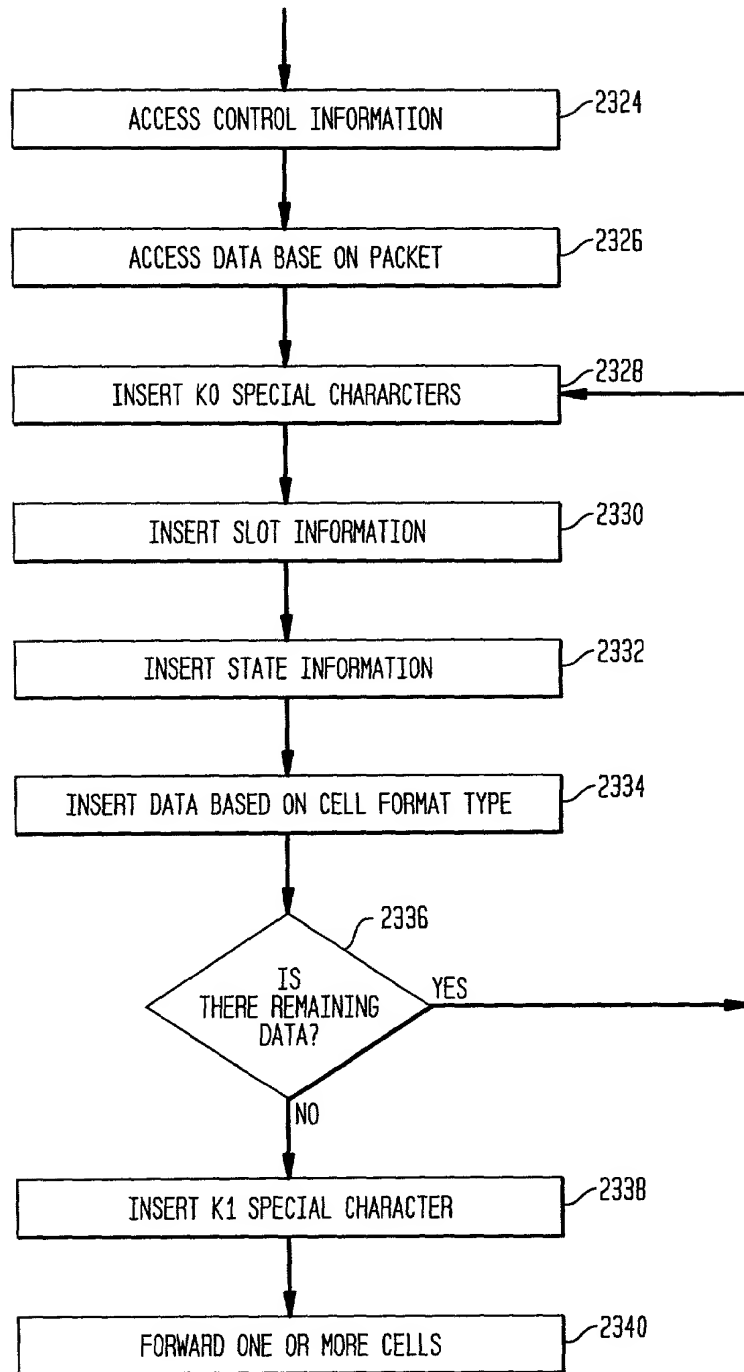


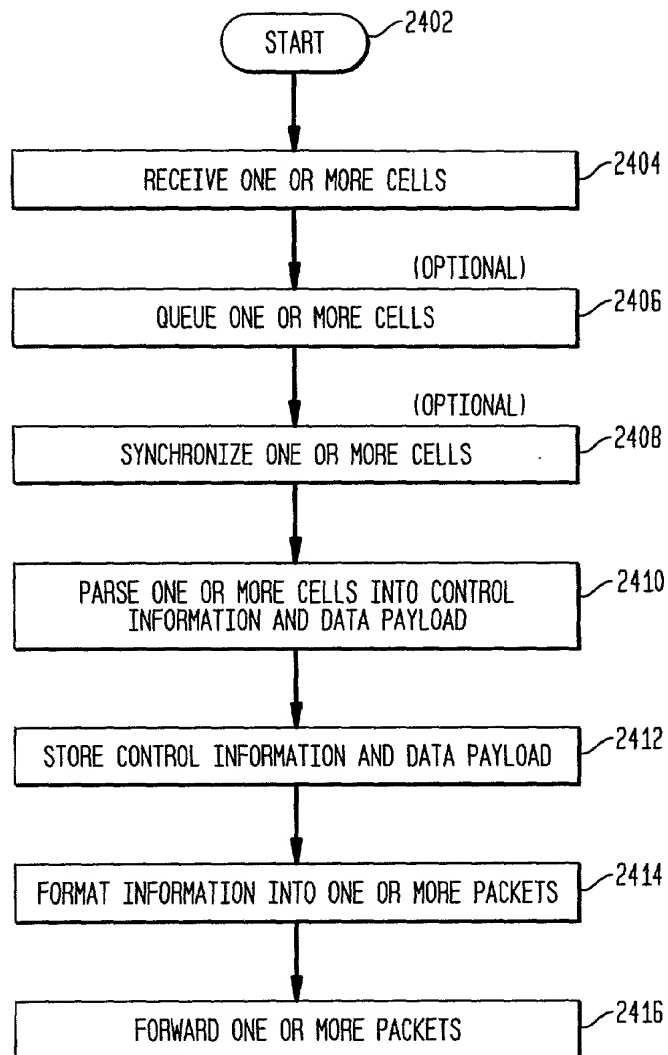
FIG. 23B

FROM 2322



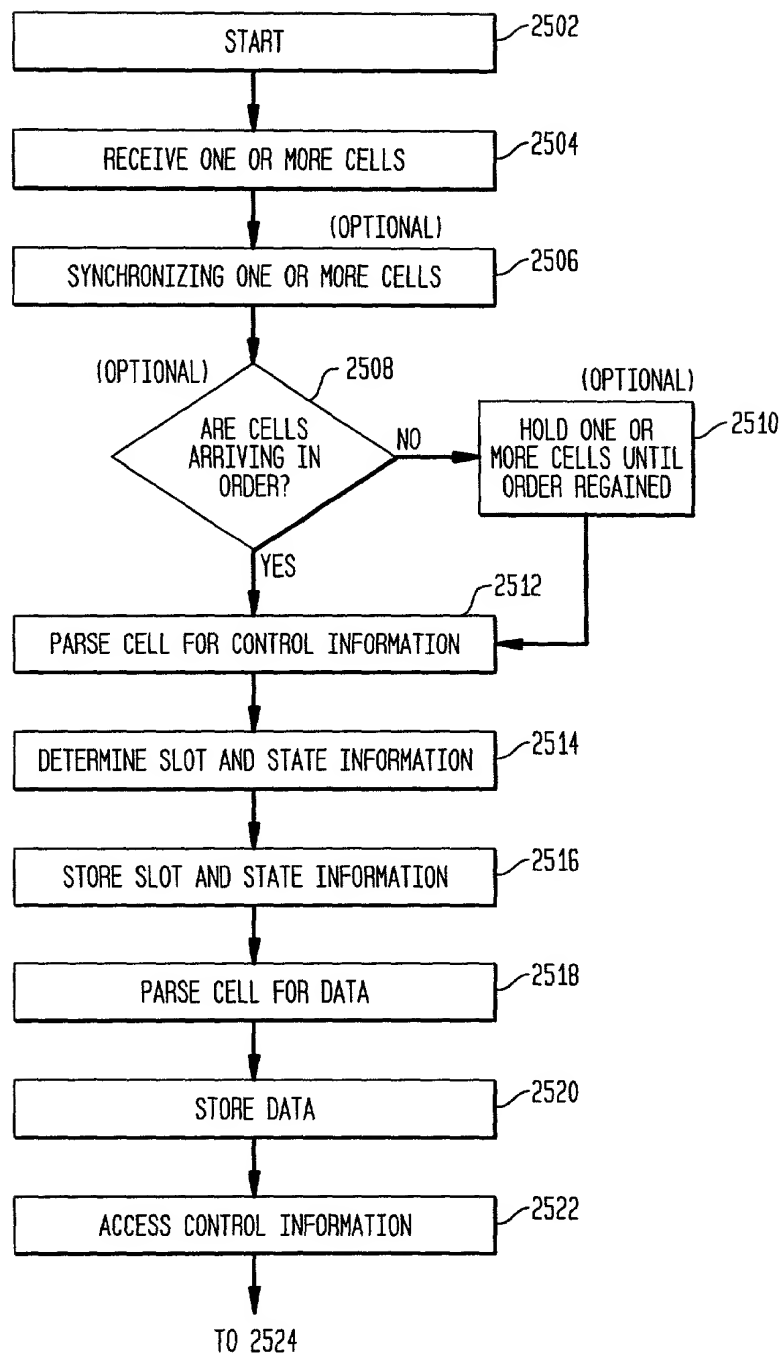
0998065 "11601

FIG. 24



0998066 11101

FIG. 25A



0998066 "11501

FIG. 25B

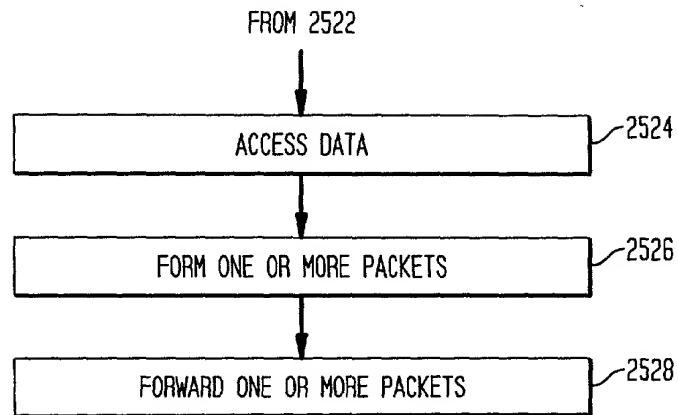


FIG. 26

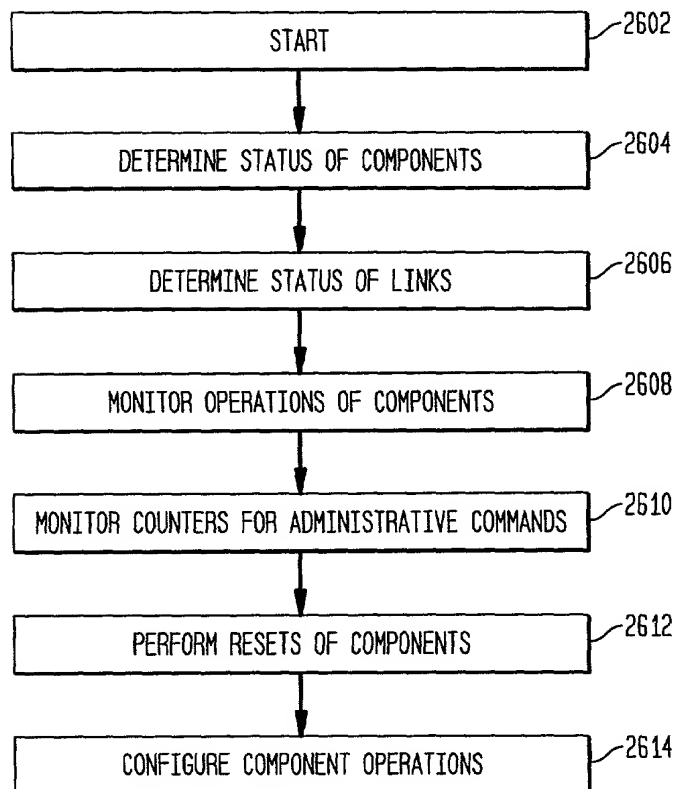
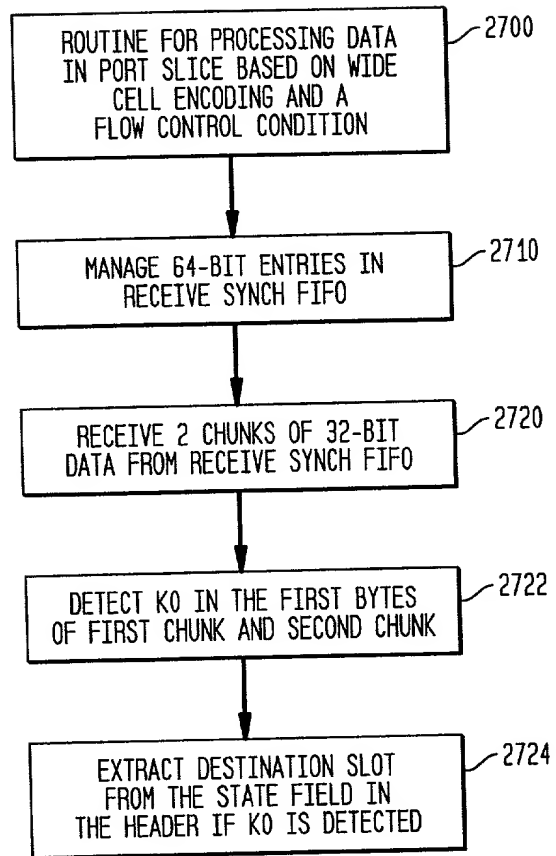


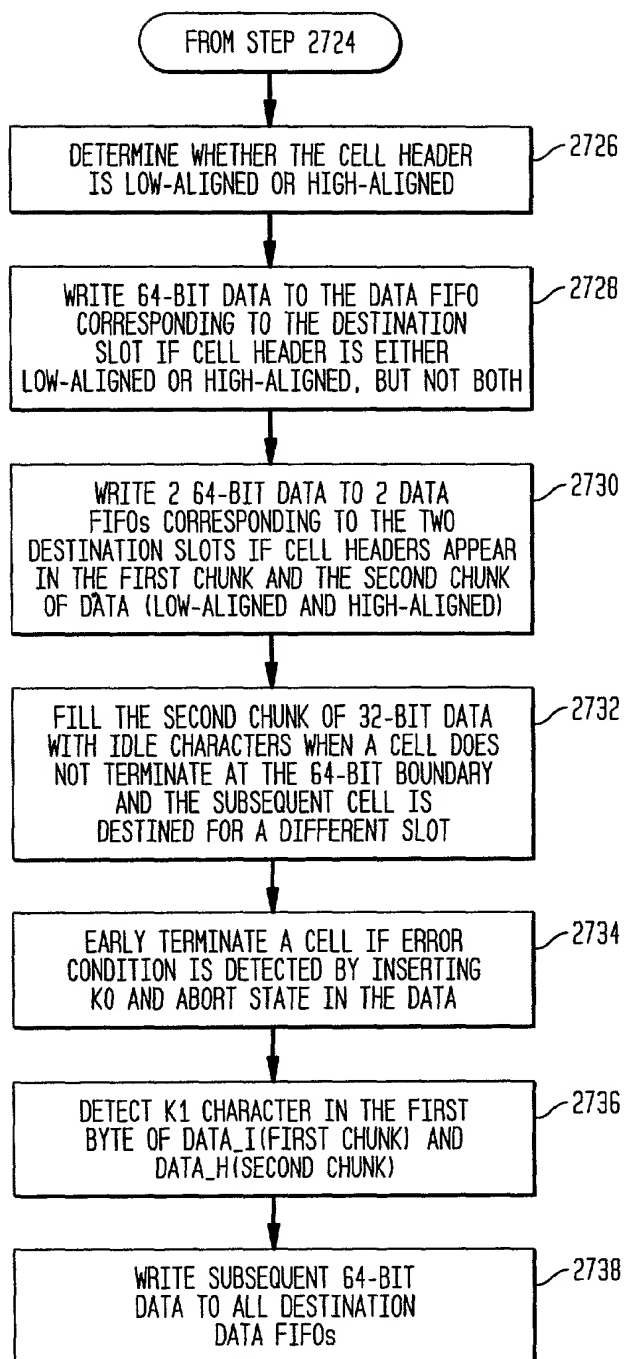
FIG. 27A



0998306 11601

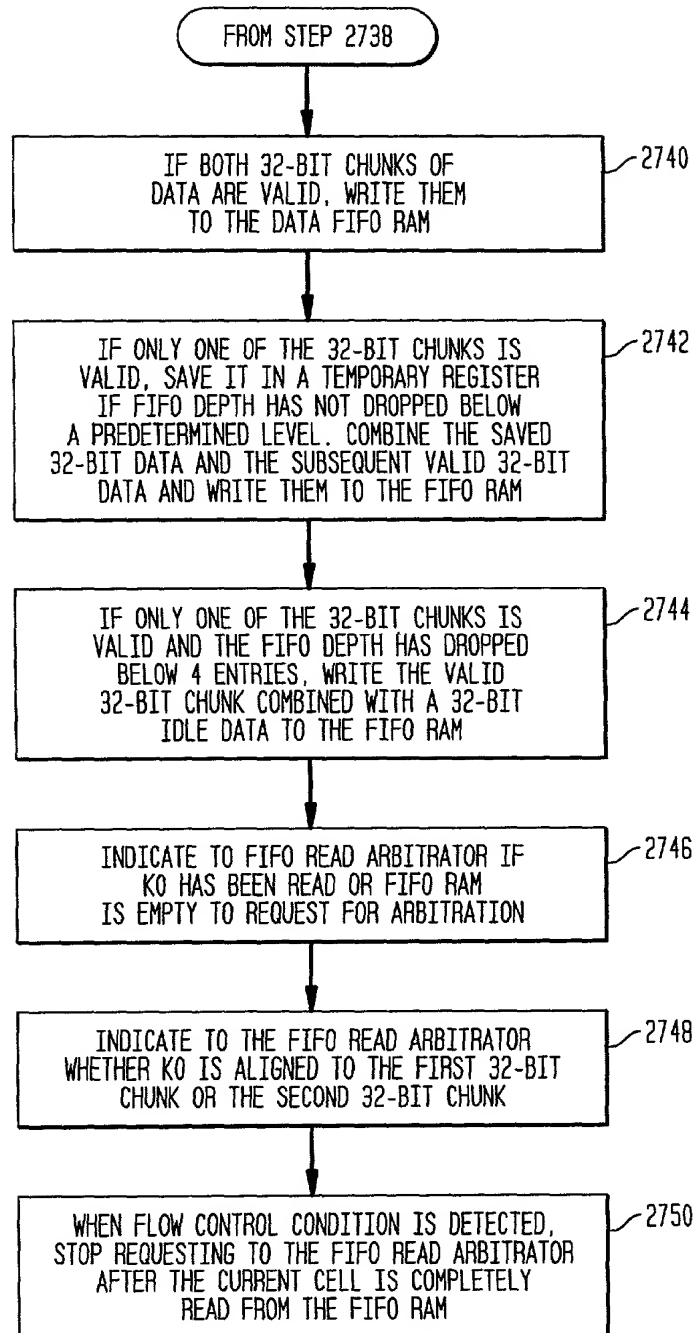


FIG. 27B



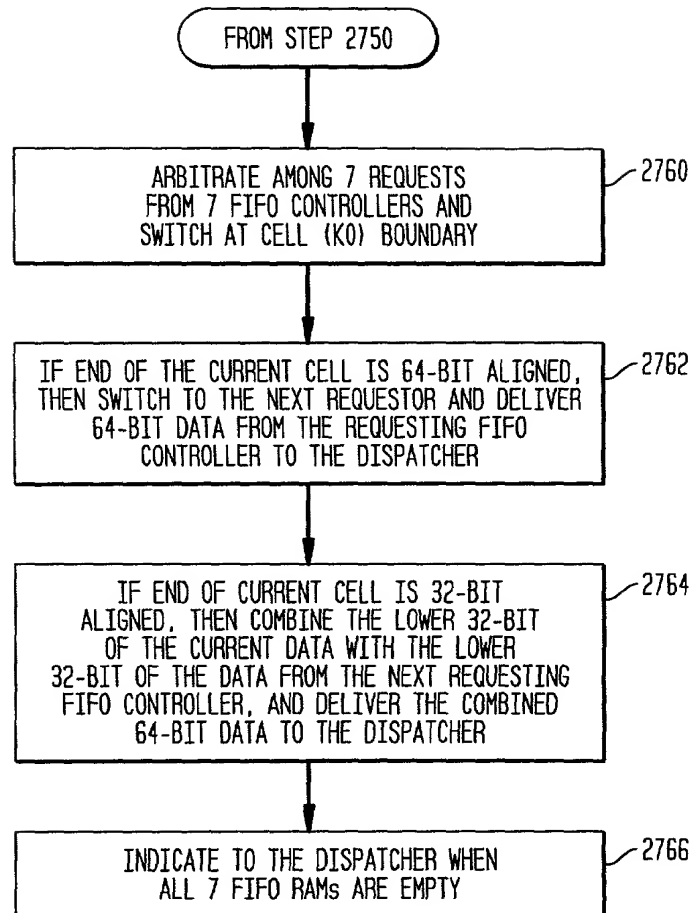
0988066-11501

FIG. 27C



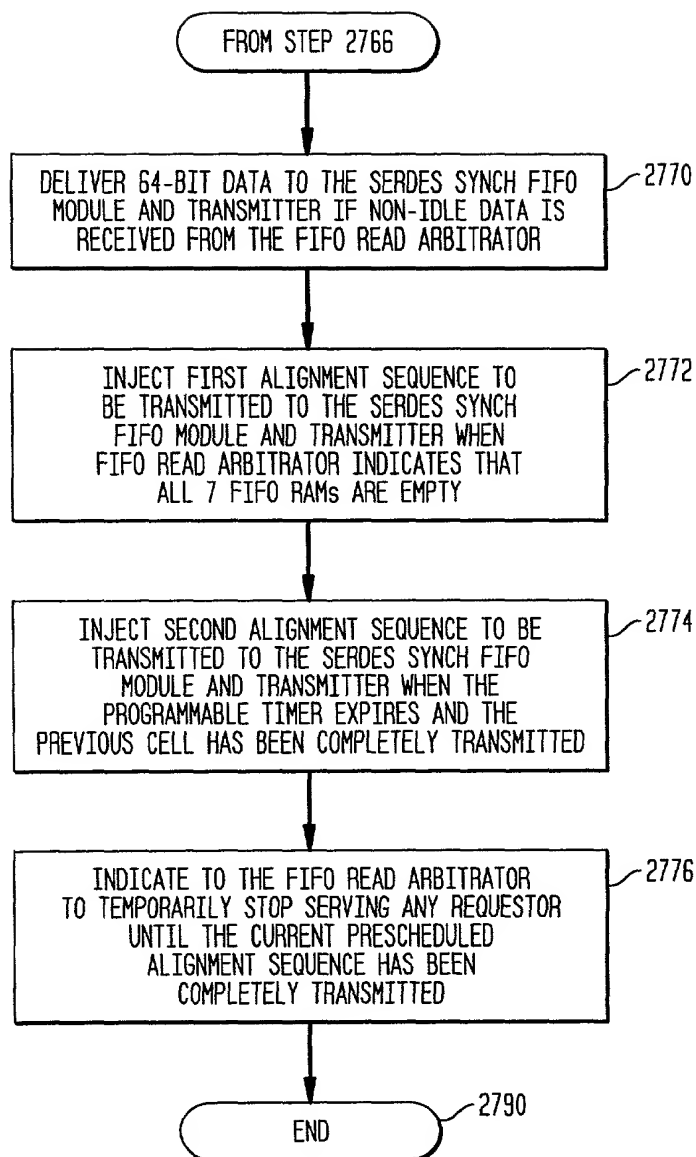
09988066 "111601"

FIG. 27D



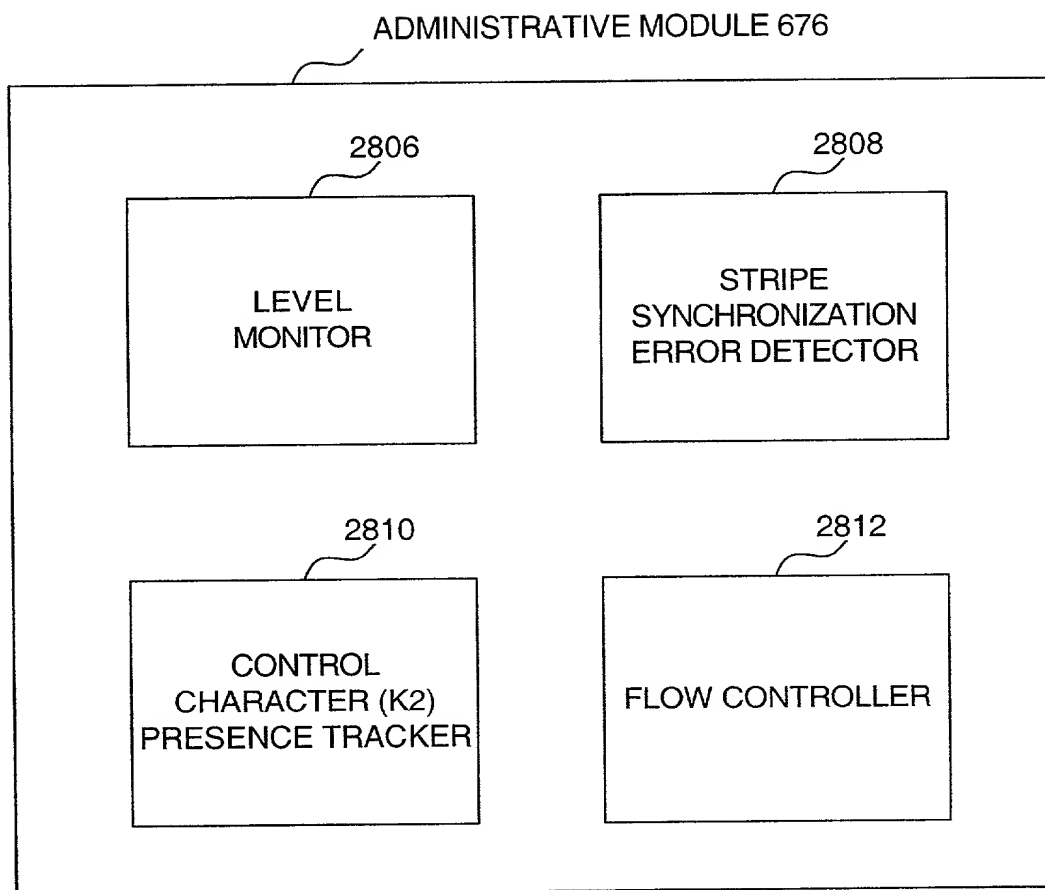
0998066 "111601

FIG. 27E



09988066 111601

**2800A**



**FIG. 28A**

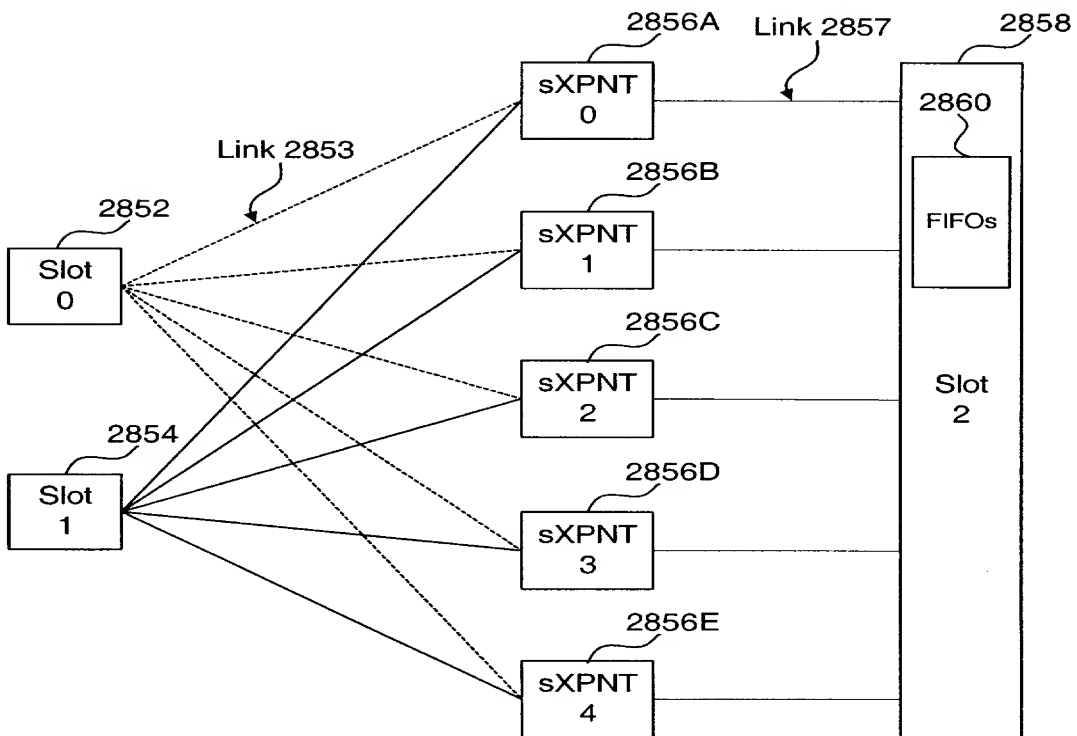


FIG. 28B

```

graph TD
    2900([Routine for Maintaining Synchronization  
of Striped Cell Traffic]) --> 2902[Send a Common Control Character in Striped Cells in  
all Lanes for a Predetermined Number of Cycles]
    2902 --> 2904[Evaluate Common Control Characters Received  
in Stripe Receive Synchronization Queues]
    2904 --> 2906{In-Synch  
Condition Detected  
?}
    2906 -- No --> 2908[Generate Error  
Message or Other  
Administrative Signal]
    2906 -- Yes --> 2910[Return to Step 2902 (Either  
Periodically or in Response to  
Administrative Control Command)]

```

FIG. 29

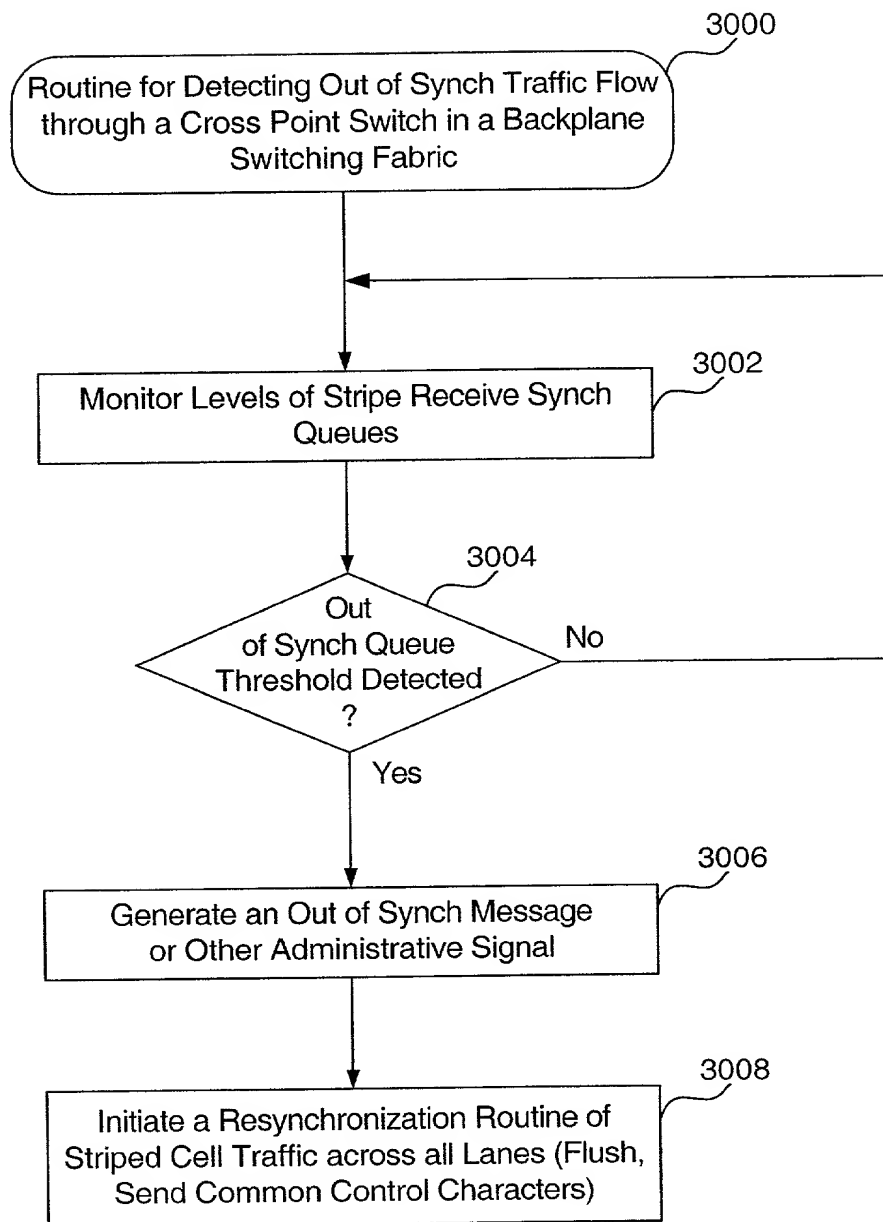
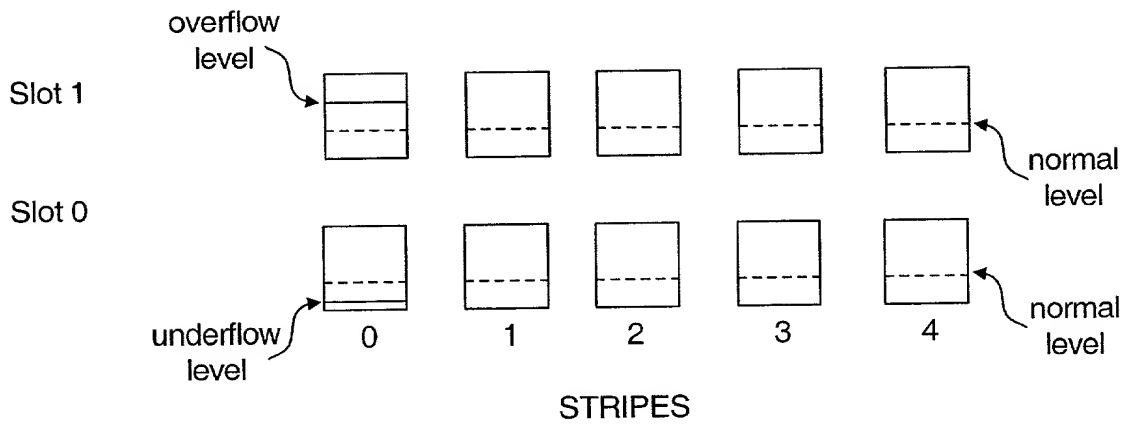


FIG. 30





Link 2853 Error Condition

FIG. 31

3200A

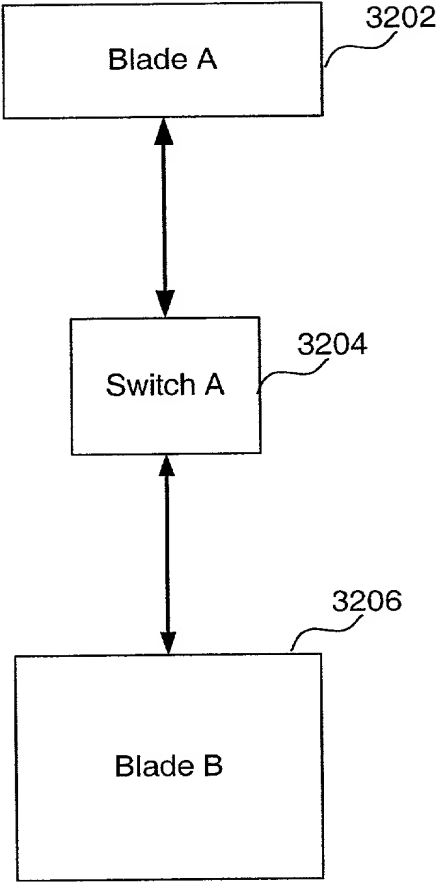
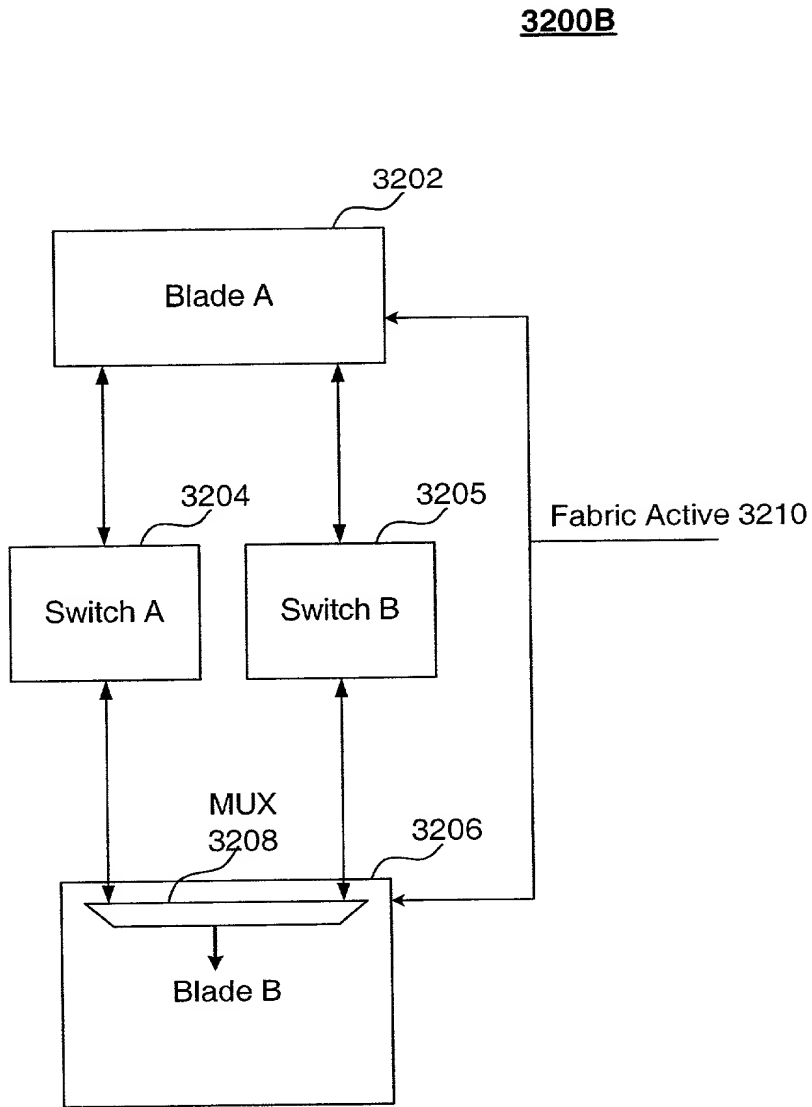


FIG. 32A



**FIG. 32B**

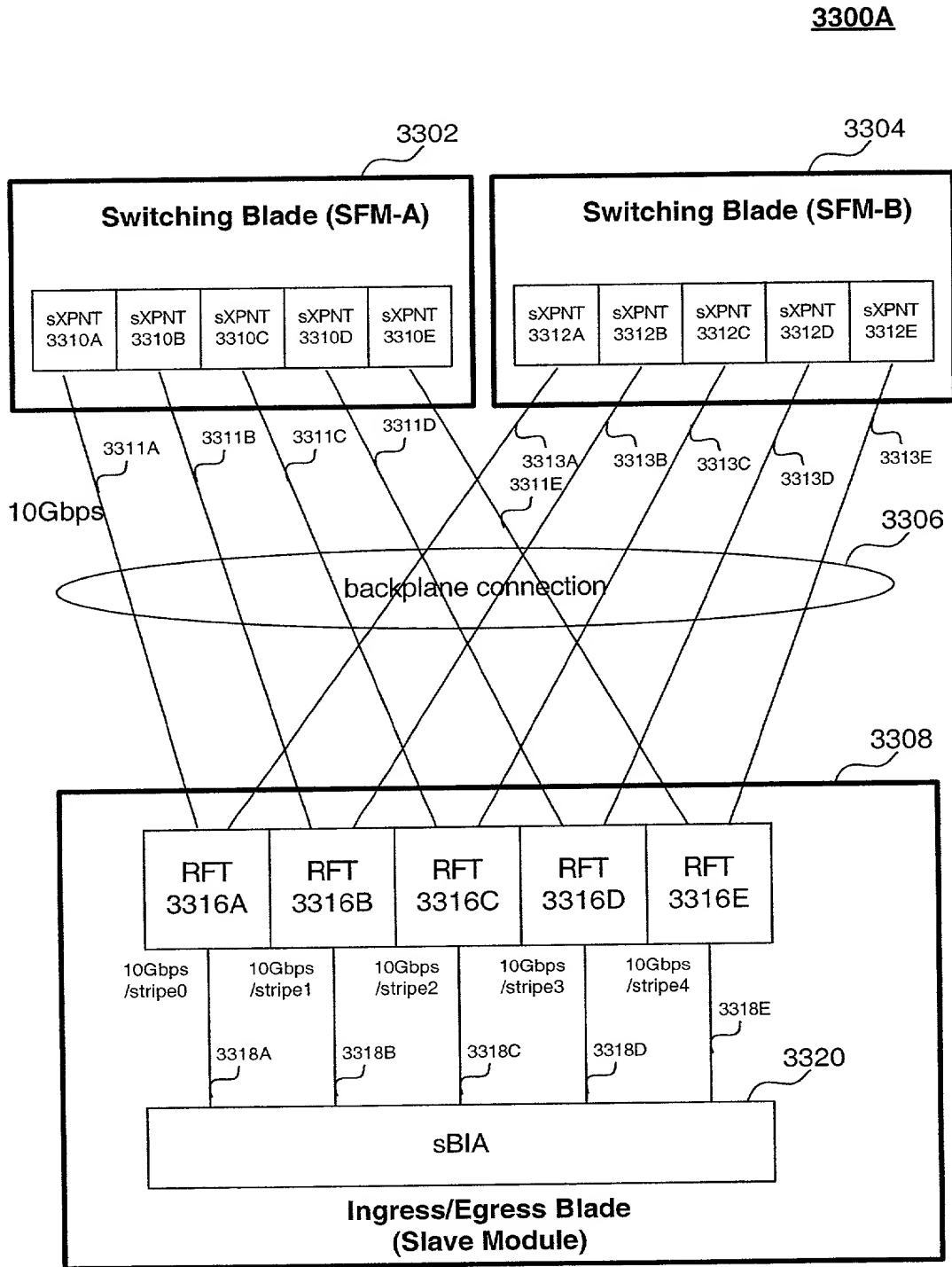
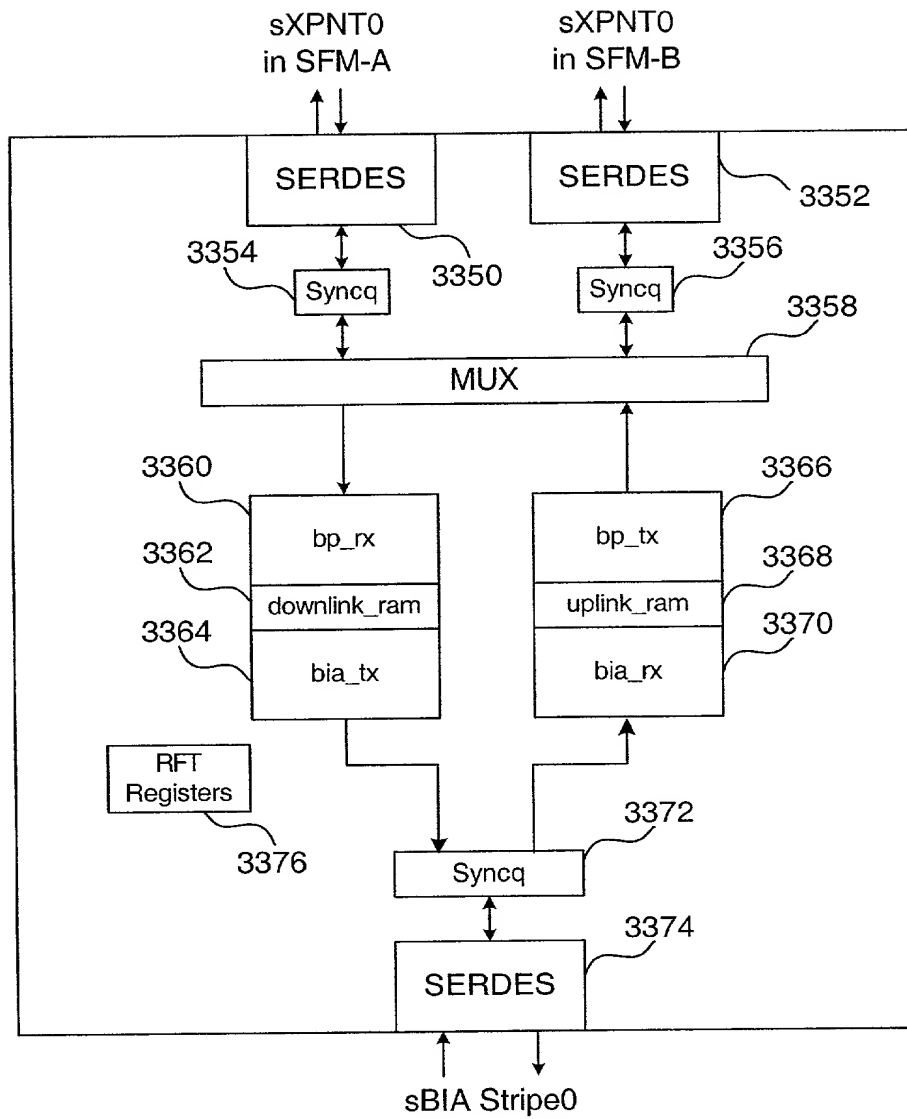


FIG. 33A

**3300B**



**FIG. 33B**

3400A

	Stripe 1				Stripe 2				Stripe 3				Stripe 4				Stripe 5			
cycle	L 0	L 1	L 2	L 3	L 0	L 1	L 2	L 3	L 0	L 1	L 2	L 3	L 0	L 1	L 2	L 3	L 0	L 1	L 2	L 3
1	K2	State	K2	K2	K2	State	K2	K2	K2	State	K2	K2	K2	State	K2	K2	K2	state	K2	K2

FIG. 34A

090806 11501

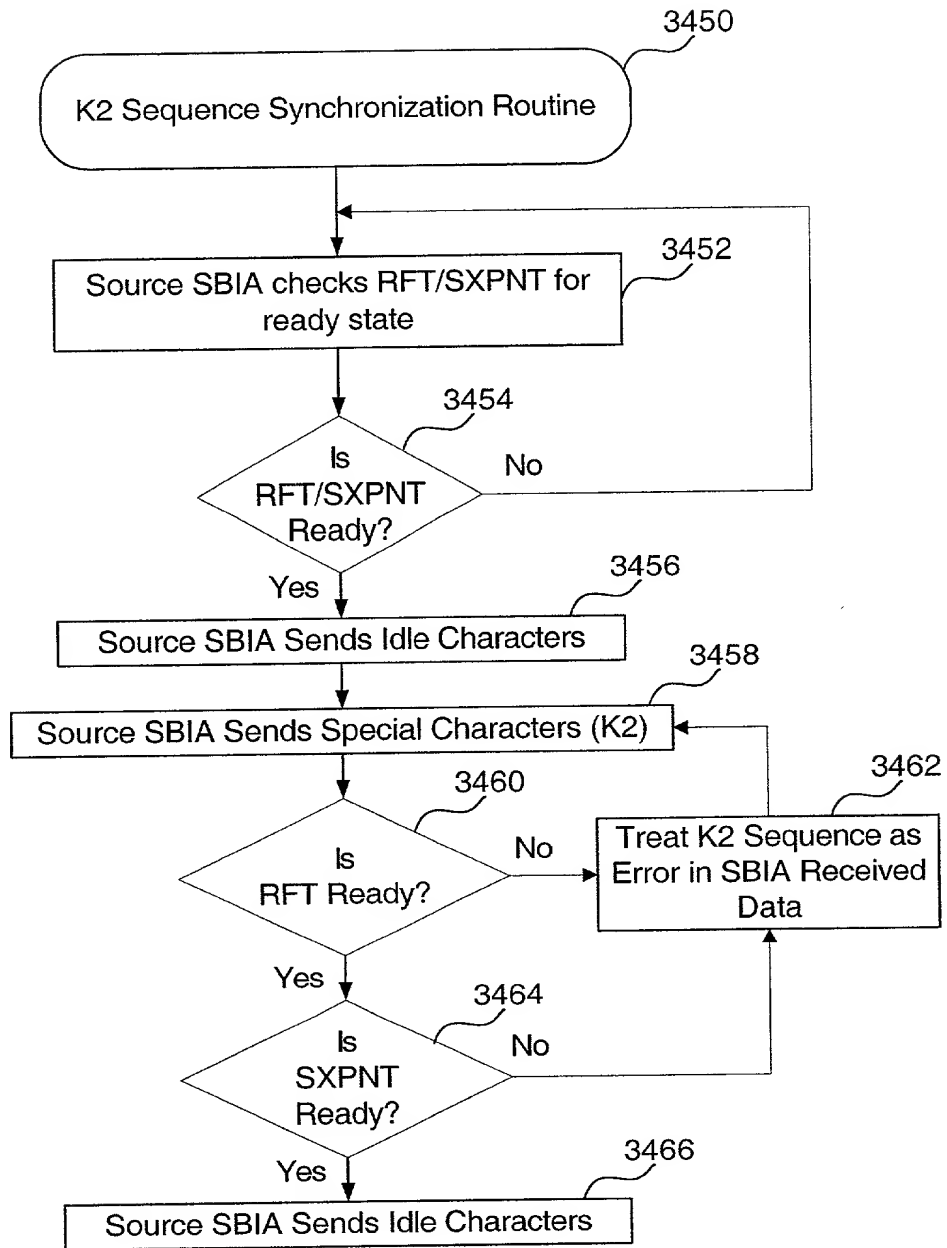


FIG. 34B

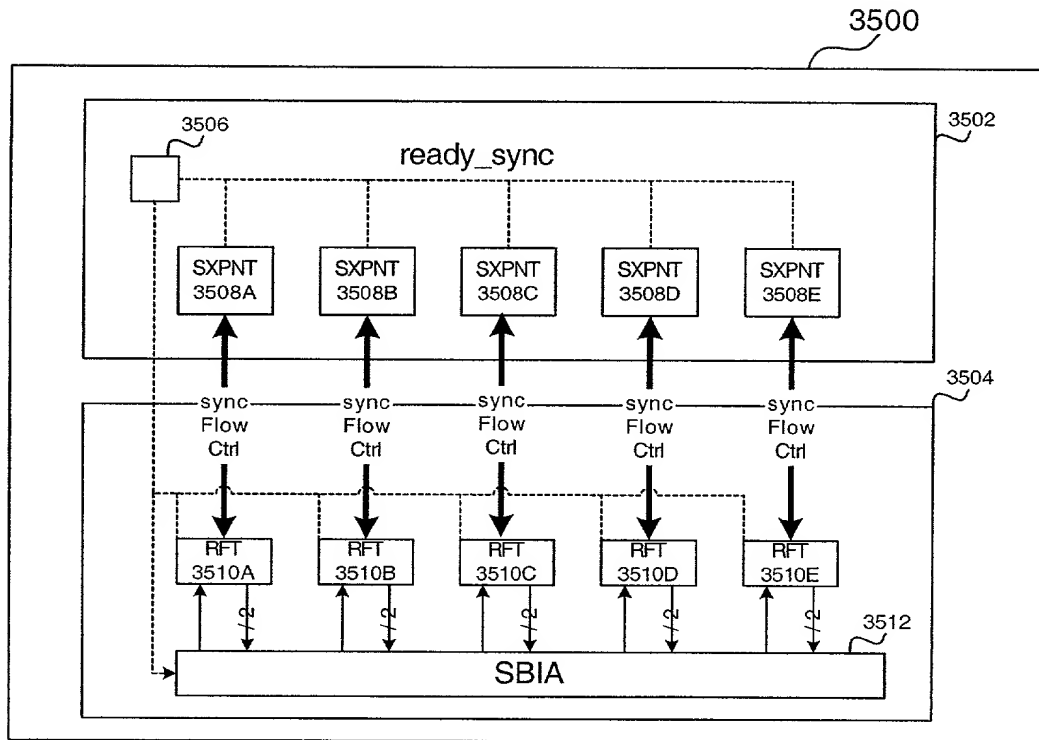
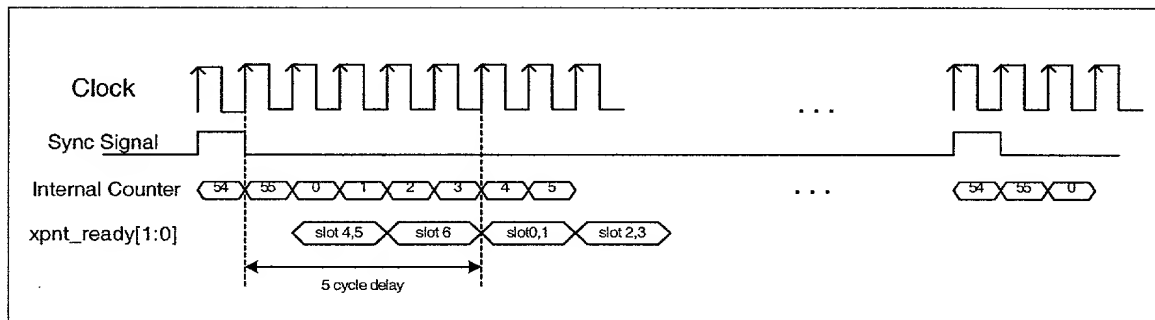


FIG. 35



**3600**



**FIG. 36**

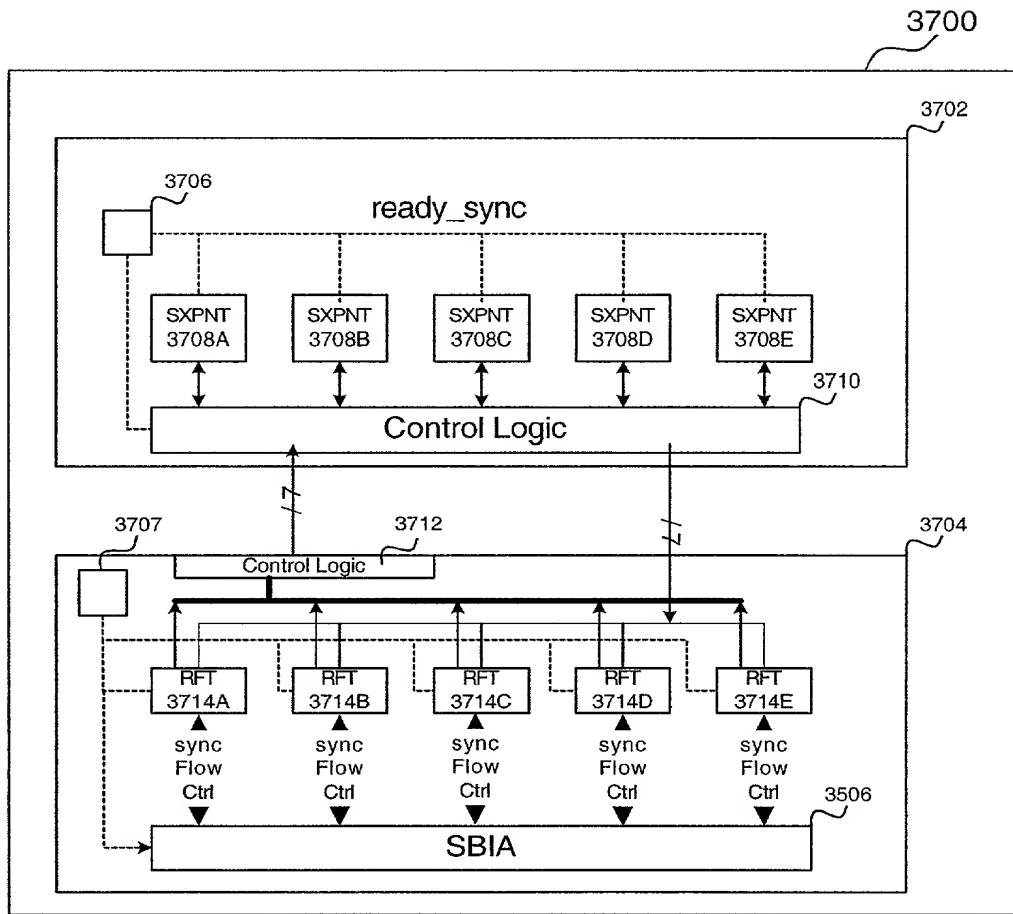


FIG. 37